Memory Devices

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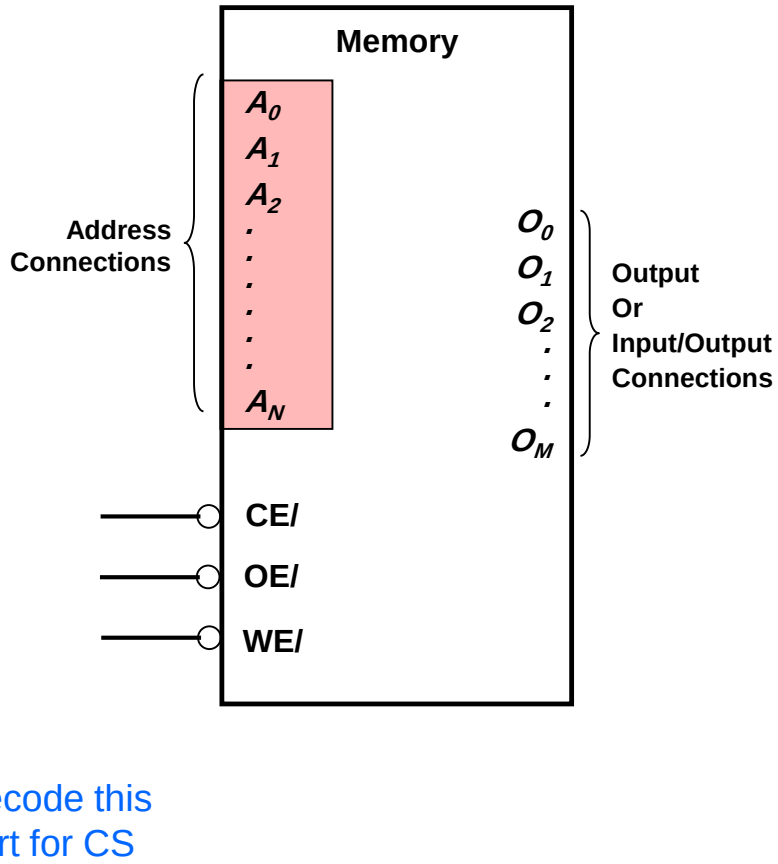
Types of Memory Devices

Two main types of memory:

- **ROM**
  - Read Only Memory
  - Non Volatile data storage (remains valid after power off)
  - For permanent storage of system software and data
  - Can be PROM, EPROM or EEPROM (Flash) memory
- **RAM**
  - Random Access Memory
  - Volatile data storage (data disappears after power off)
  - For temporary storage of application software and data
  - Can be SRAM (static) or DRAM (dynamic)

Memory Pin Connections

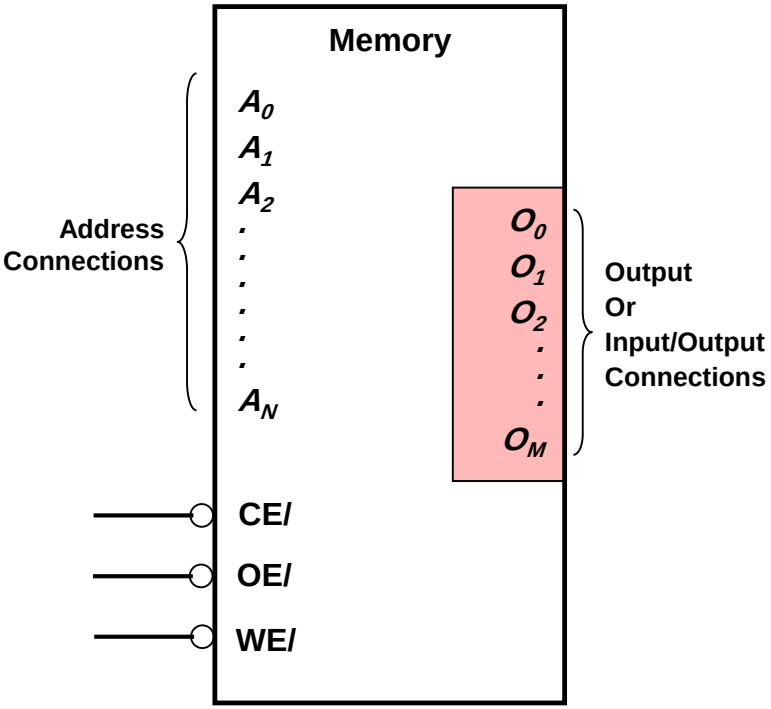
- **Address Inputs:**
  - Select the required location in memory.
  - Address lines are numbered from A_0 to as many as required to address all memory locations
  - Example: 12-bit address: A_0-A_{11}
    $\Rightarrow 2^{12}$ = 4K memory locations
  - Today's memory devices range in capacities upto 1G locations (30 address lines)
  - Example: 4K memory: 12 bits: 000H-FFFH. e.g. from 40000H to 40FFFH.



Memory Pin Connections

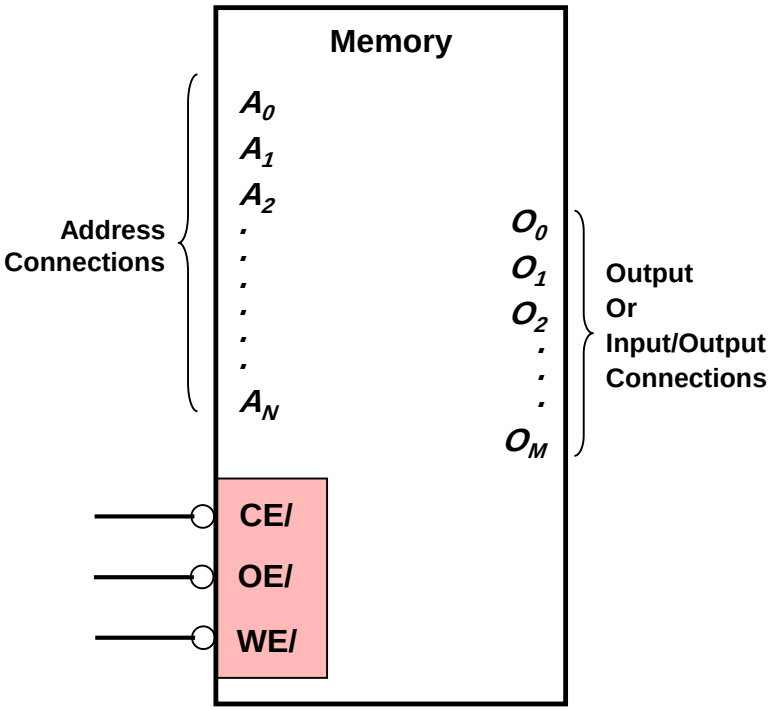
- **Data Inputs/Outputs (RAM)**
  Data Outputs (ROM)
  - Number of lines = width of data storage, usually a byte D0-D7 (M=7)
  - Wider processor data buses use multiple of such byte-wide memory devices, e.g. 64-bit

    $\Rightarrow$ 8 x 8-bit devices
  - Sometimes the total memory capacity is expressed in bits, e.g. a 64K x 8-bit = 512 Kbit



Memory Pin Connections

- **Control Inputs:**
  - **Chip Enable (CE/), or Chip Select (CS/), or simply Select (S/):** Select the memory device for READ or WRITE operations.
  - In addition, Indicate whether you want to READ or Write:
  - READ: Enable device output for READ operations (only operation on ROMs) using **OE/** or **G/.** If not enabled, output will be Hi-Z (floating)
  - WRITE: (for RAM only) Enable device for writing using **WE/** input. Should not be active simultaneously with #OE
  - Some memory devices have one READ/WRITE control: R/#W



Memory Organization

- Many memory device are 8-bits in width.
- A 4K x 8 memory contains 4,096 (4K) memory locations, each containing 8-bits
- A 16M x 4 memory has 16 M memory locations, each being 4-bits wide
- A 512M byte DDR* memory card for your PC is organized as a 64M x 8 bytes. It contains eight 64M x 8 bit memory devices

* Double Data Rate, SDRAM with data transfer at both clock edges

Read Only Memory Devices

Many Types of read only memory: (Programming getting easier…)

- **ROM**
  - Device permanently programmed in factory by manufacturer
  - Must be large number (≈10,000 pieces) to justify cost
  - Once manufactured, can not be erased or reprogrammed

- **PROM**
  - **Programmable** ROM (Programmed once)
  - When number of devices is too small to justify high factory programming cost
  - Programmed in a PROM programmer that burns fuse kinks
  - Once programmed, can not be erased for reprogramming
  - Changes? Throw away and program another one!

Read Only Memory Devices (Cont'd)

- **EPROM**
  - **E**rasable **P**rogrammable **ROM** (Programmed many)
  - Used when contents need to be changed, e.g. during the development phase of a product
  - Reprogrammed in an EPROM programmer
  - Erased by exposure to UV light for say 20 minutes before reprogramming

- **EEPROM**
  - **E**lectrically **E**rasable **P**rogrammable ROM (Programmed many … and in situ)
  - Other names: RMM (Read mostly memory), NOVRAM (Non Volatile RAM), Flash memory
  - Erasing and reprogramming is made so easy (and in situ) that it can be thought of as **writing** (hence RAM, but with data not volatile**)**
  - But erasing/writing takes longer time than writing into a RAM, but this is OK since it is less frequent
  - Applications: BIOS, Memory for digital cameras and MP3 audio players, USB storage devices

EPROM

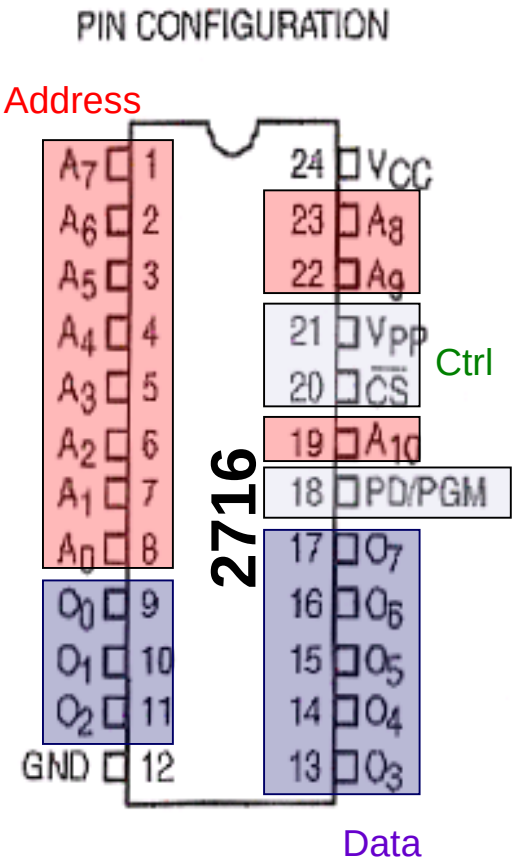
- 2K x 8 read only memory

  1 bit + 10 bits = 11 Address inputs

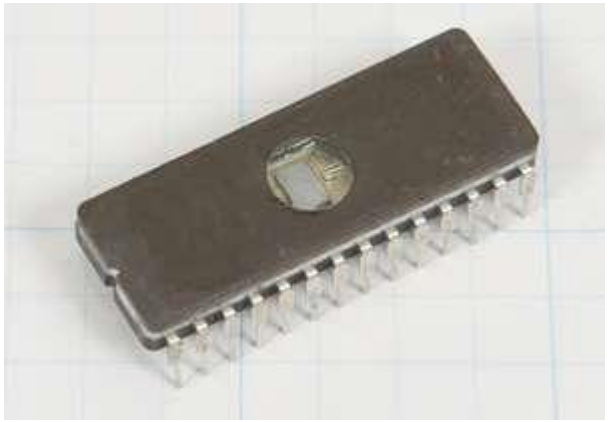
  8 Data outputs

- Members of the 27XXXX family:
  - 2704 : 512 x 8
  - 2708 : 1K x 8
  - 2716 : 2K x 8
  - 2732 : 4K x 8
  - 2764 : 8K x 8
  - 27128 : 16K x 8
  - 27256 : 32K x 8
  - 27512 : 64K x 8
  - 271024 : 128K x 8

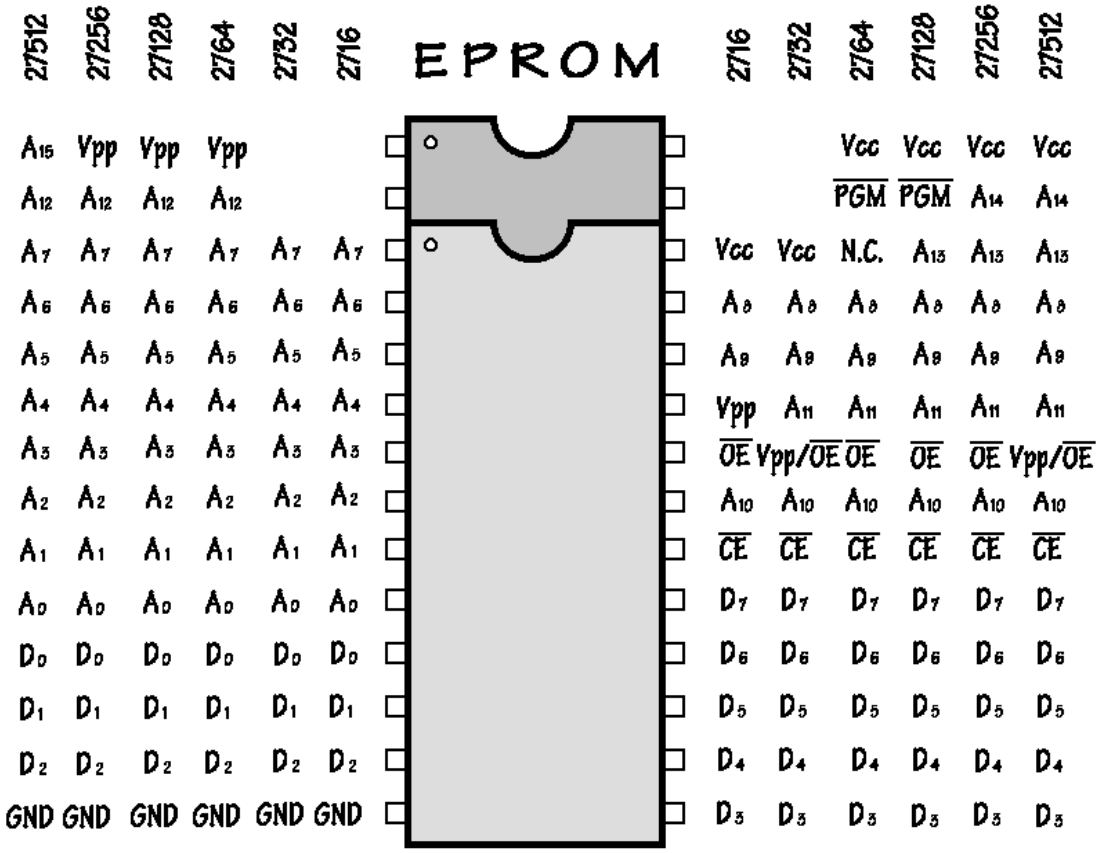
= Memory capacity in K bits



EPROM (2764A)

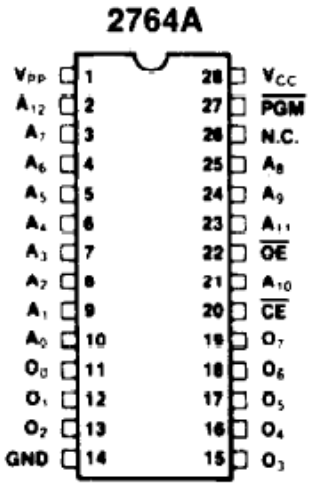


A_0-A_{12}	Addresses
CE/	Chip Enable
OE/	Output Enable
O_0-O_7	Outputs
PGM/	Program
N.C.	Not Connected

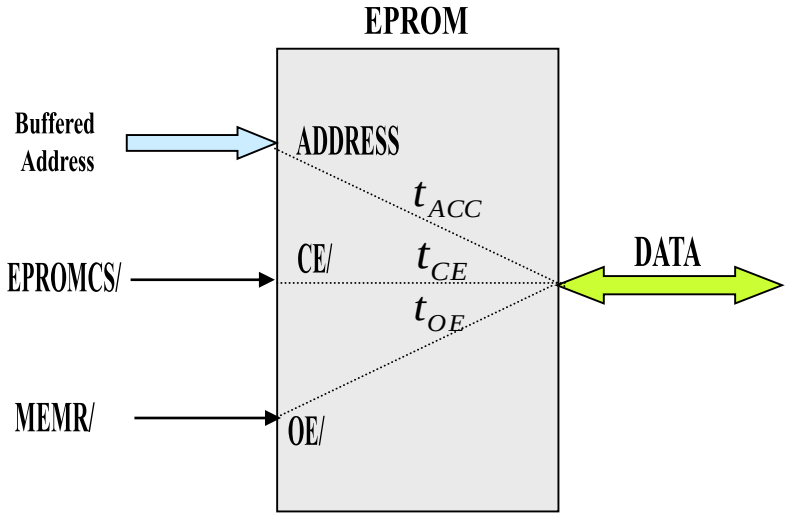


EPROM Timing Parameters

27512 27C512	27256 27C256	27128A 27C128	2732A	2716
A_{15}	V_{PP}	V_{PP}		
A_{12}	A_{12}	A_{12}		
A_7	A_7	A_7	A_7	A_7
A_6	A_6	A_6	A_6	A_6
A_5	A_5	A_5	A_5	A_5
A_4	A_4	A_4	A_4	A_4
A_3	A_3	A_3	A_3	A_3
A_2	A_2	A_2	A_2	A_2
A_1	A_1	A_1	A_1	A_1
A_0	A_0	A_0	A_0	A_0
O_0	O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2	O_2
GND	GND	GND	GND	GND

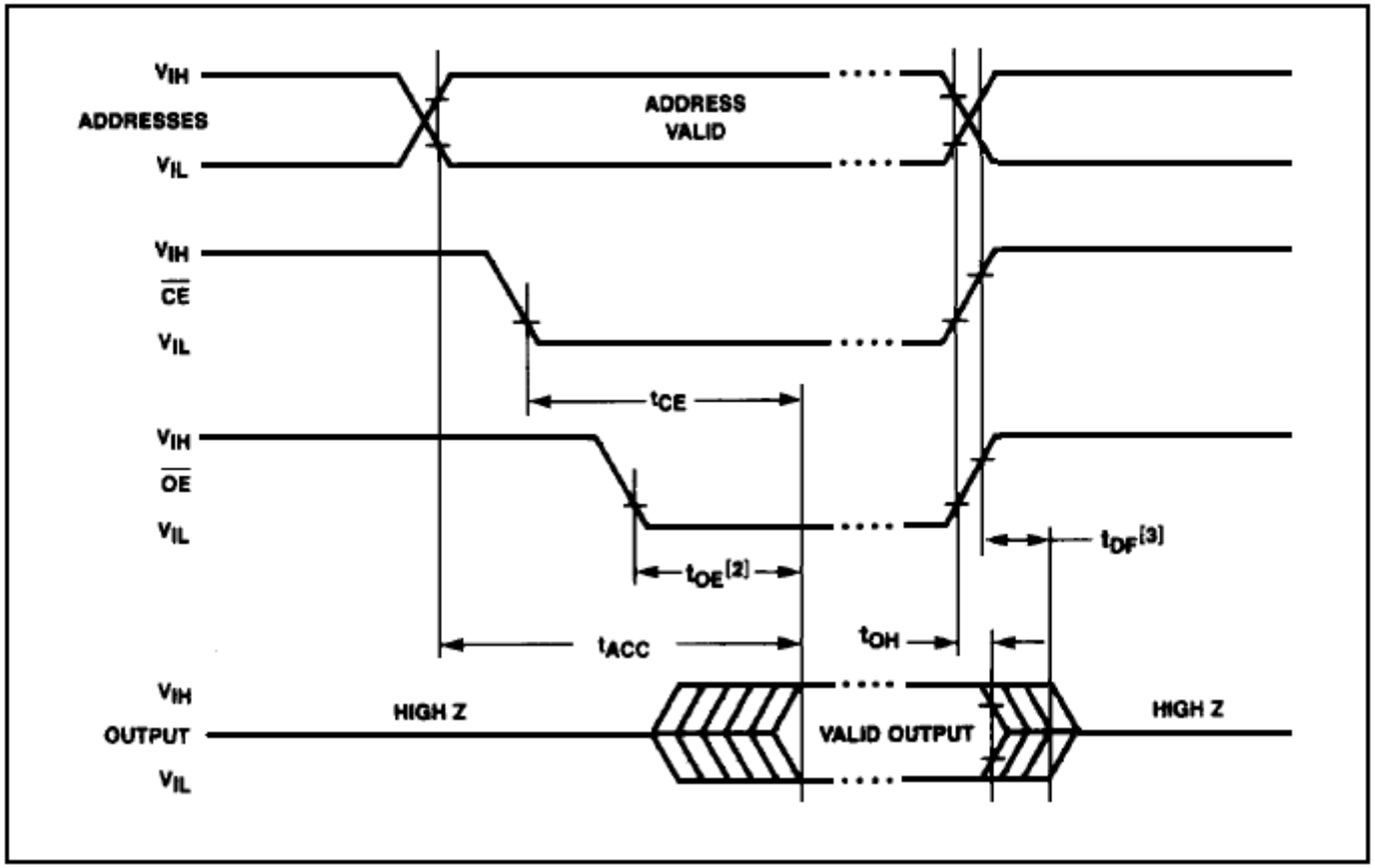


2716	2732A	27128A 27C128	27256 27C256	27512 27C512
		V_{CC} PGM	V_{CC} A_{14}	V_{CC} A_{14}
V_{CC}	V_{CC}	A_{13}	A_{13}	A_{13}
A_8	A_8	A_8	A_8	A_8
A_9	A_9	A_9	A_9	A_9
V_{PP}	A_{11}	A_{11}	A_{11}	A_{11}
$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$
A_{10}	A_{10}	A_{10}	A_{10}	A_{10}
$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
O_7	O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3	O_3



EPROM Timing Parameters (2764A)

A.C. WAVEFORMS



EPROM Timing Parameters (2764A)

READ OPERATION

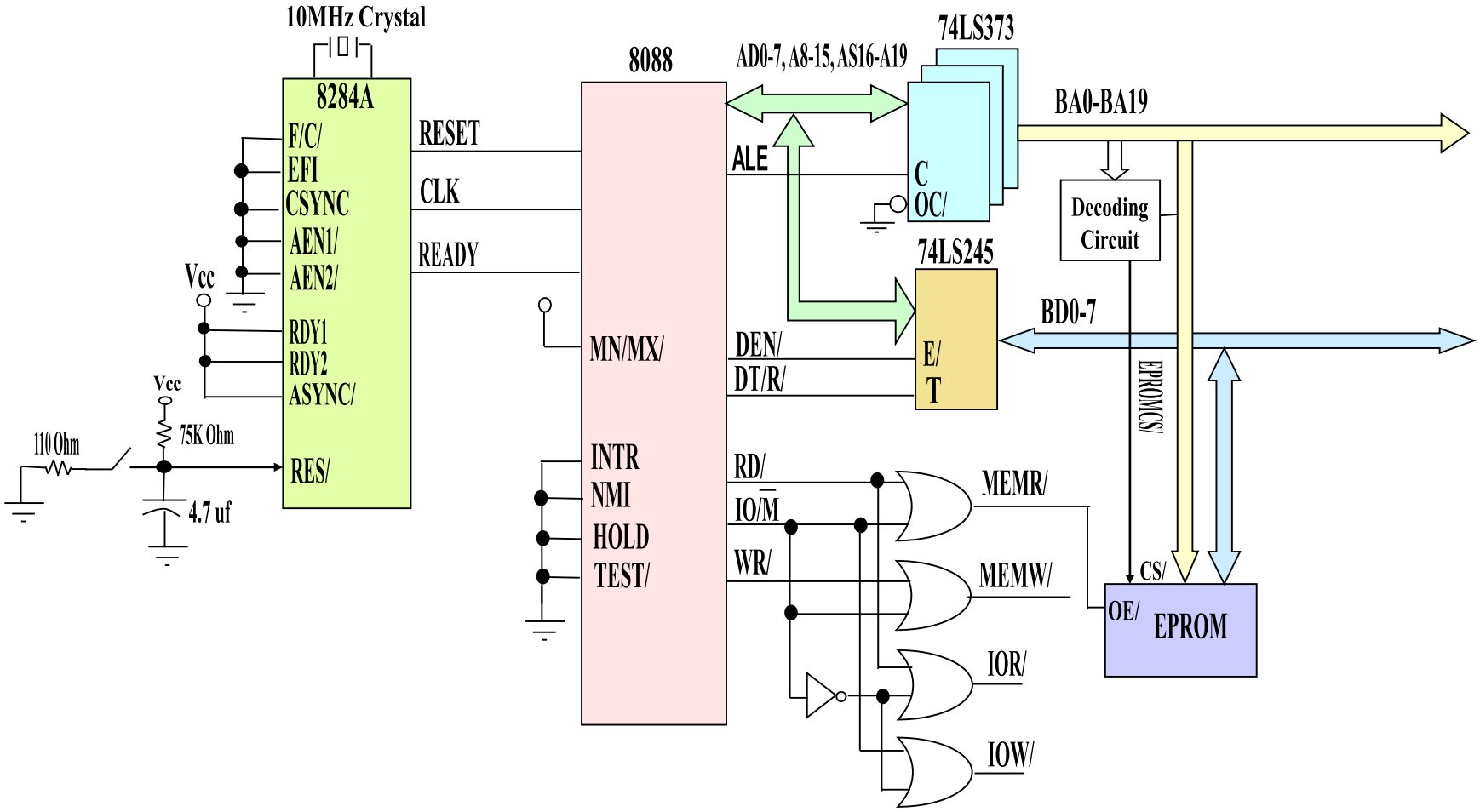
D.C. CHARACTERISTICS $0°C \le T_A \le +70°C$

Symbol	Parameter	Limits			Conditions
		Min	Max	Unit	
I_{LI}	Input Load Current		10	µA	V_{IN} = 0V to V_{CC}
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = 0V to V_{CC}
I_{PP}(2)	V_{PP} Current Read		5	mA	V_{PP} = 5.5V
I_{SB}	V_{CC} Current Standby		35	mA	$\overline{CE}$ = V_{IH}
I_{CC}(2)	V_{CC} Current Active		75	mA	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
V_{IL}	Input Low Voltage	−0.1	+0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} + 1	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −400 µA
V_{PP}(2)	V_{PP} Read Voltage	3.8	V_{CC}	V	V_{CC} = 5.0V ± 0.25V

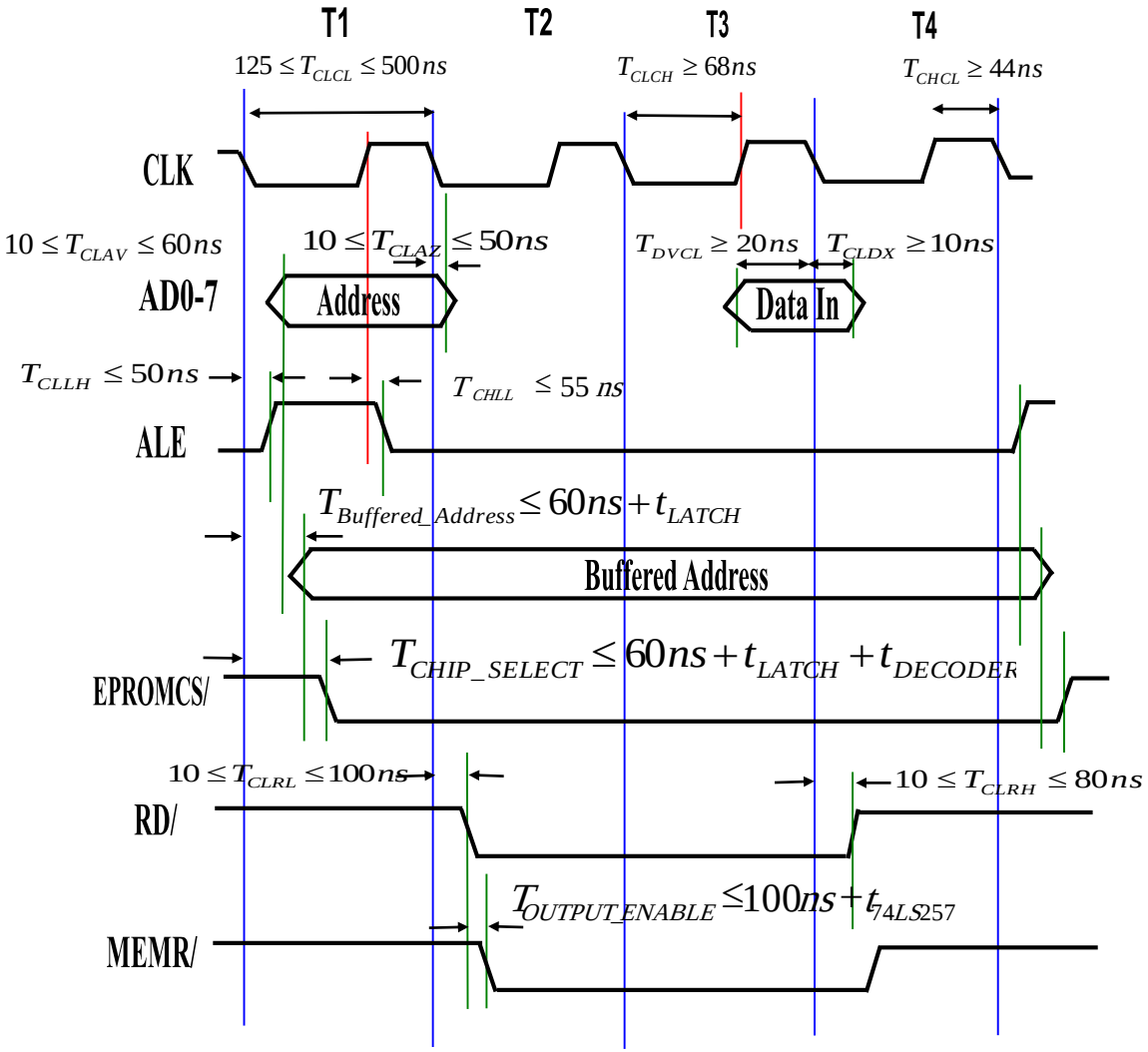
A.C. CHARACTERISTICS $0°C \le T_A \le +70°C$

Versions(4)	V_{CC} ± 5%	2764A-1		2764A-2		2764A		Unit	Test Conditions
	V_{CC} ± 10%			2764A-20		2764A-25			
Symbol	Parameter	Min	Max	Min	Max	Min	Max		
t_{ACC}	Address to Output Delay		180		200		250	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
t_{CE}	$\overline{CE}$ to Output Delay		180		200		250	ns	$\overline{OE}$ = V_{IL}
t_{OE}	$\overline{OE}$ to Output Delay		65		75		100	ns	$\overline{CE}$ = V_{IL}
t_{DF}(3)	$\overline{OE}$ High to Output Float	0	55	0	55	0	60	ns	$\overline{CE}$ = V_{IL}
t_{OH}(3)	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	0		0		0		ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}

Example: Interfacing EPROM to 8088-2



Example: Interfacing EPROM to 8088-2

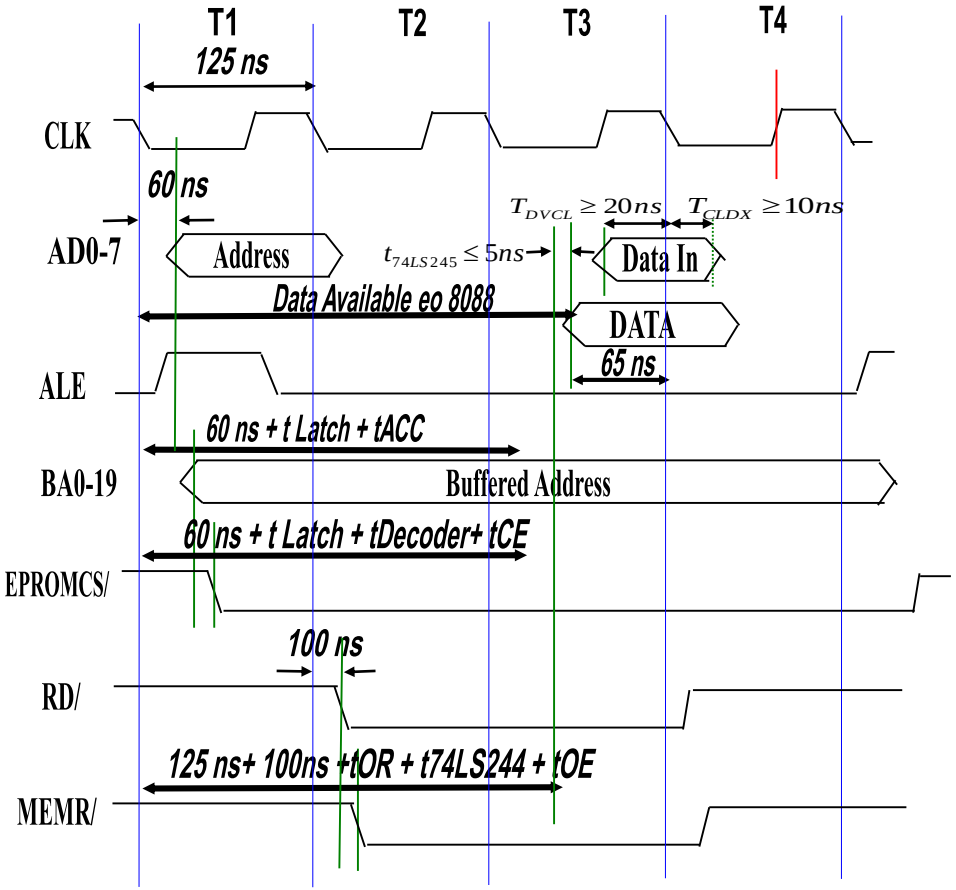


Example: Interfacing EPROM to 8088-2

$$EPROM\_OUTPUT = MAX\{60ns + t_{LATCH} + t_{ACC},\ 60ns + t_{LATCH} + t_{Decoder} + t_{CE},\ t_{T1} + 100ns + t_{OR} + t_{74LS244} + t_{OE}\}$$

$$Data\_Avaiable\_to\_8088 = t_{74LS245} + MAX\{60ns + t_{LATCH} + t_{ACC},\ 60ns + t_{LATCH} + t_{Decoder} + t_{CE},\ t_{T1} + 100ns + t_{OR} + t_{74LS244} + t_{OE}\}$$

2764A-2 is Compatible with 8088-2 (Zero Wait State)



RAM Memory Devices

- Writing is needed more often than with EEPROMs
  $\rightarrow$ should be easier and faster.

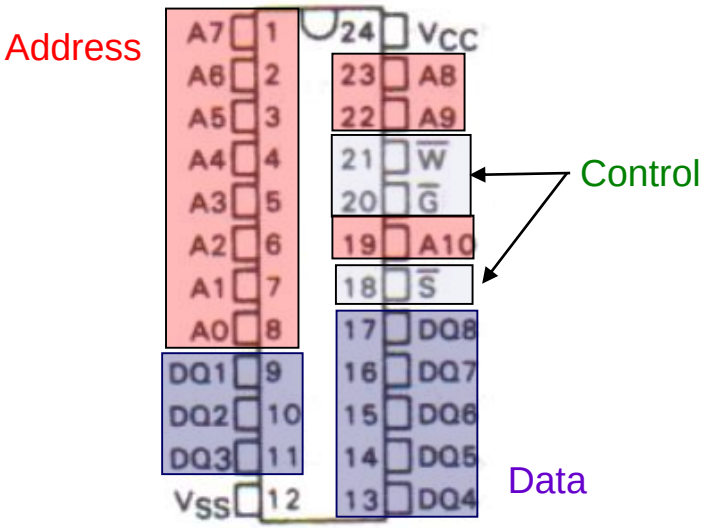
- Two main types of RAM:
  - **Static RAM**
  - **Dynamic RAM**

Static RAM (SRAM)

- A relatively complex cell circuit (several transistors per bit storage)
- That is why static RAM devices are more expensive and are typically smaller in capacity compared to dynamic RAM (A given # of transistors available on a chip gives fewer memory locations)
- Faster than dynamic RAMs, speeds down to 1 ns access time are now possible
- Used for high speed cache memories
- It is rarely the case that a large computer RAM uses only static memory type

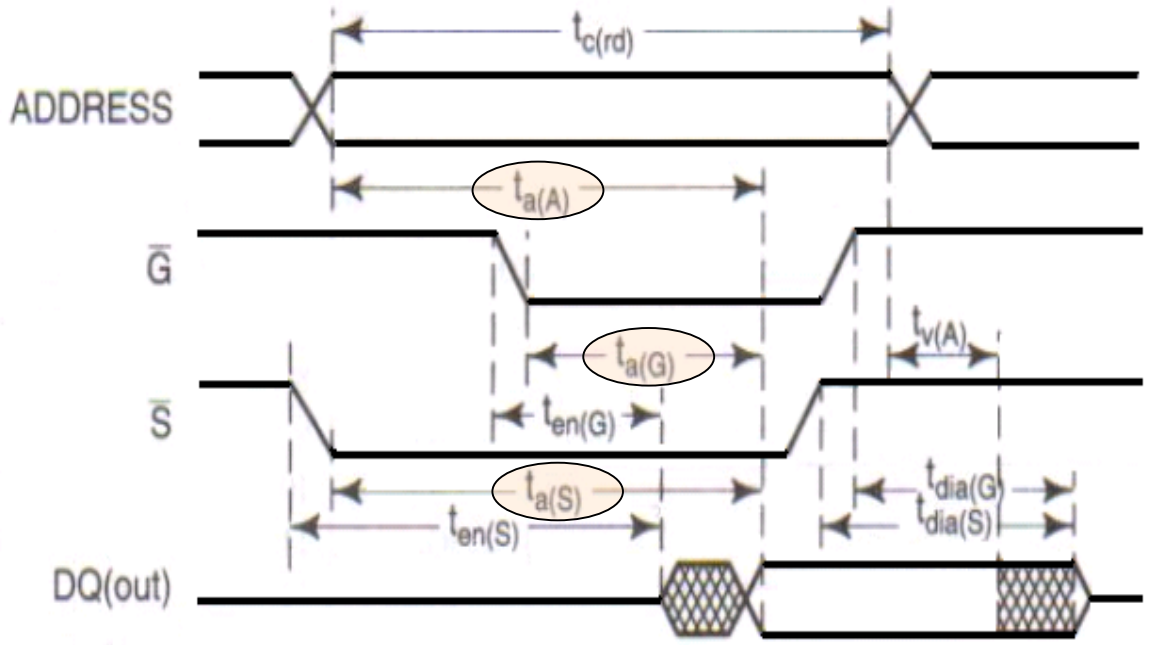
Static RAM Example: the 4016

- 2K x 8 RAM (same size as the 2716)
- 11 bit address (A0-A10), 8-bit data (DQ1-DQ8): Data in/Data out
- Also produced with the numbers 2016, 4116, 6116, and 9028
- CS/ is S/, OE/ (RD/) is G/, WR/ is W/
- Range of speeds: access times in the range 120 ns to 250 ns (various chip versions, e.g. TMS4016-25 has 250 ns access time)
- All can be interfaced with the 8088/8086 without wait states



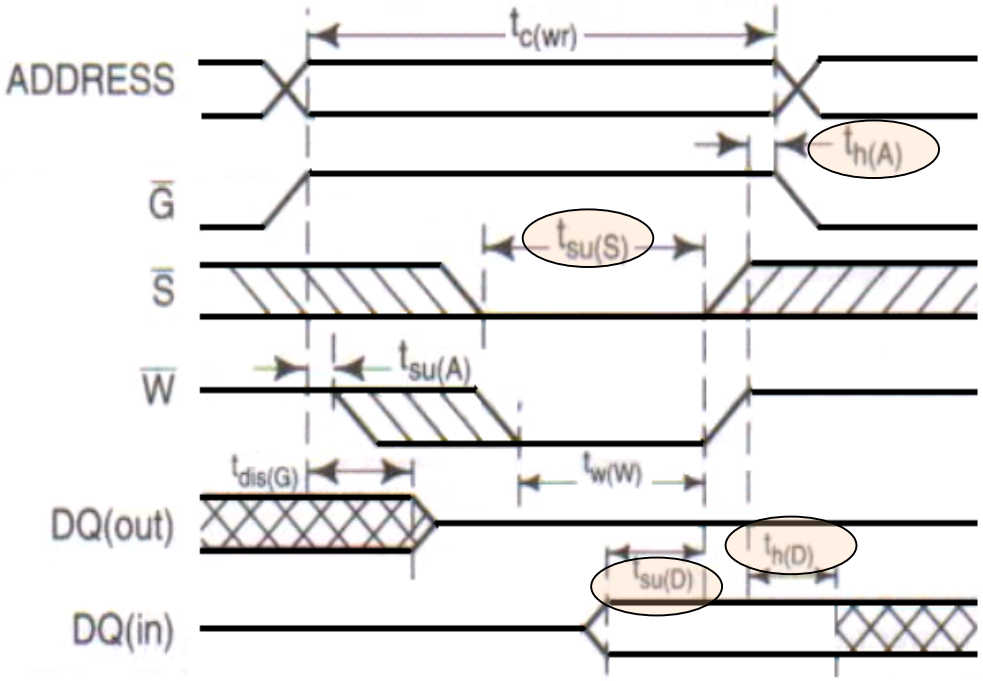
PIN NOMENCLATURE	
A0 – A10	Addresses
DQ1 – DQ8	Data In/Data Out
$\overline{G}$	Output Enable
$\overline{S}$	Chip Select
V_{CC}	+5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

Static RAM Example: the 4016



Timing Waveform of Read Cycle

Static RAM Example: the 4016



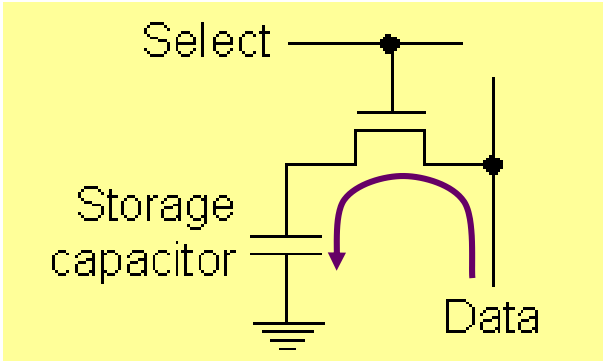
Timing Waveform of Write Cycle

Dynamic RAM (DRAM)

- Unlike static RAM, data is store as a voltage (charge) across a capacitor
- Charge of course leaks with time, and data needs to be refreshed (re-written) every say 2-4 ms
- Recent devices usually organized as XX K x 1 bit, largest 1G x 1
- Advantages:
  - Simpler cell circuit
  - Larger capacities

    While Largest SRAM ≈ 8 Mbits,

    Largest DRAM ≈ 1024 Mbits
  - Lower cost than SRAM



- Disadvantages:
  - Slower access times (e.g. 20 ns vs 1 ns)
  - Needs refreshing: e.g. every 4 ms max (added complexity)

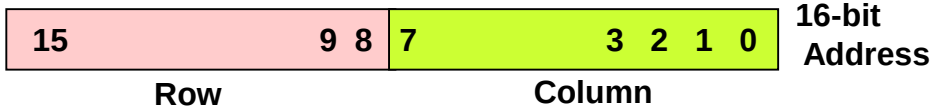
    But not that bad!:

    Occurs during normal reads and writes. Also special hidden refresh cycles occurring simultaneously with other memory accesses (cycle stealing). Dedicated DRAM refresh controller chips available.
  - Large storage capacity → large address inputs → large number of chip pins required → Need for chip pin multiplexing (added complexity)

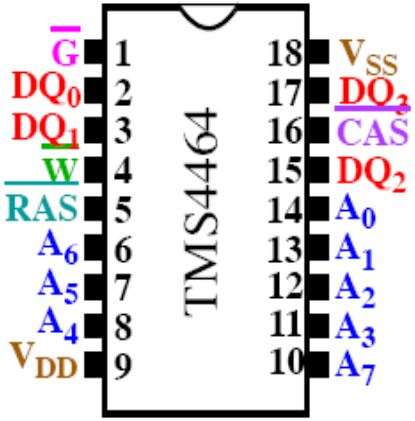
Dynamic RAM (DRAM)

- 64 K x 4 DRAM

  6 bits + 10 bits = 16 bits memory address
- But only 8 address lines on the chip!
- 16 address lines split into row and column 8-bit parts:



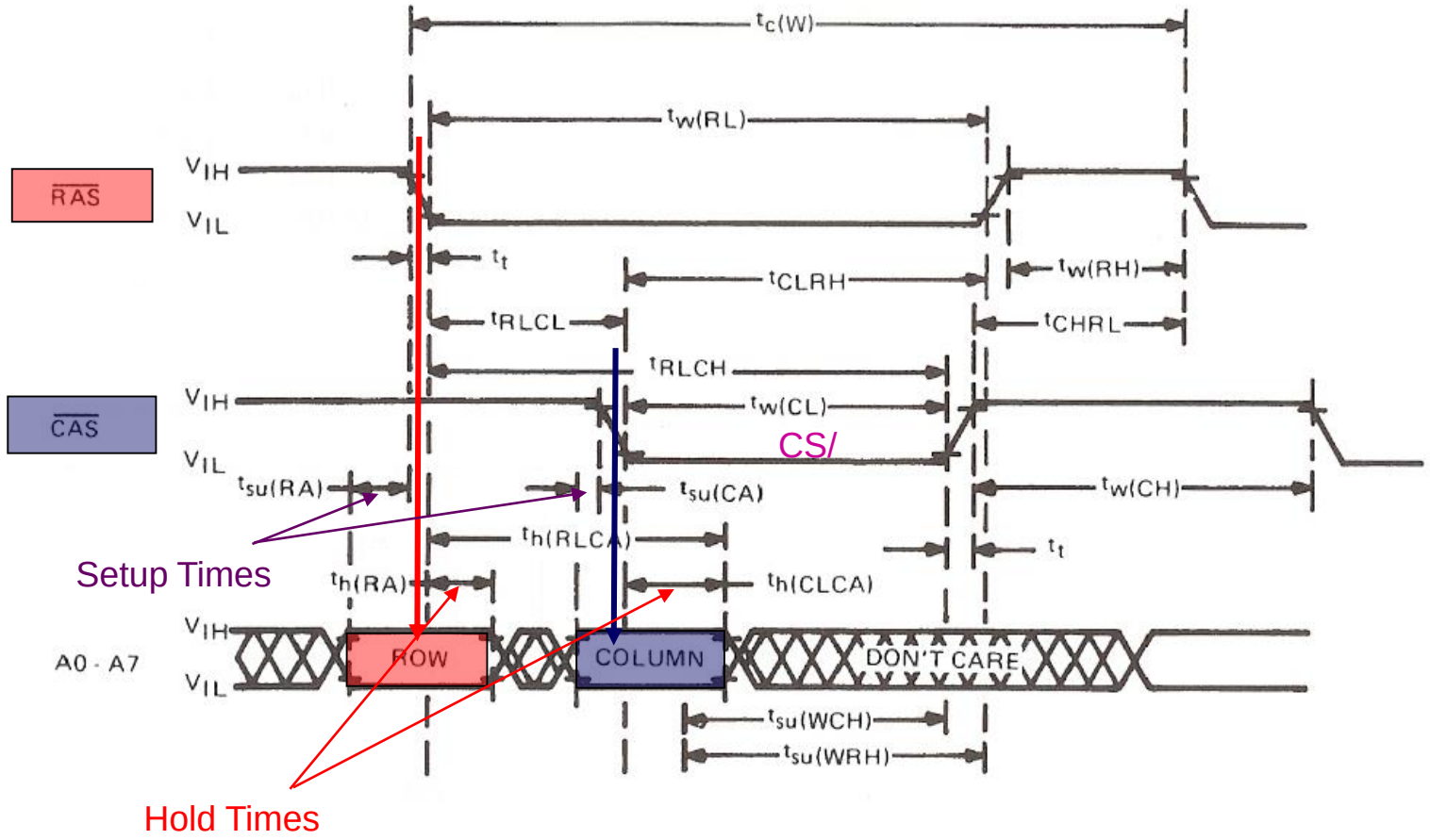
- Most significant 8-bit row address is first latched in using the RAS/ input (Row Address Select)
- Then 8-bit column address is latched in using the CAS/ input
- This loads the 16-bit address into a latch on the chip
- CAS/ also acts as CS/
- OE/ is G/, WE/ is W/, CS/ is CAS/
- Access time: Fastest version is 100 ns?



TI TMS4016 (64K ×4

Pin(s)	Function
A_0-A_7	Address
DQ_0-DQ_3	Data In/Data Out
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable

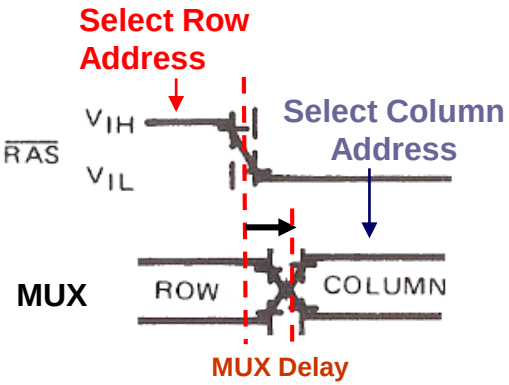
Timing Diagram for Address Strobing



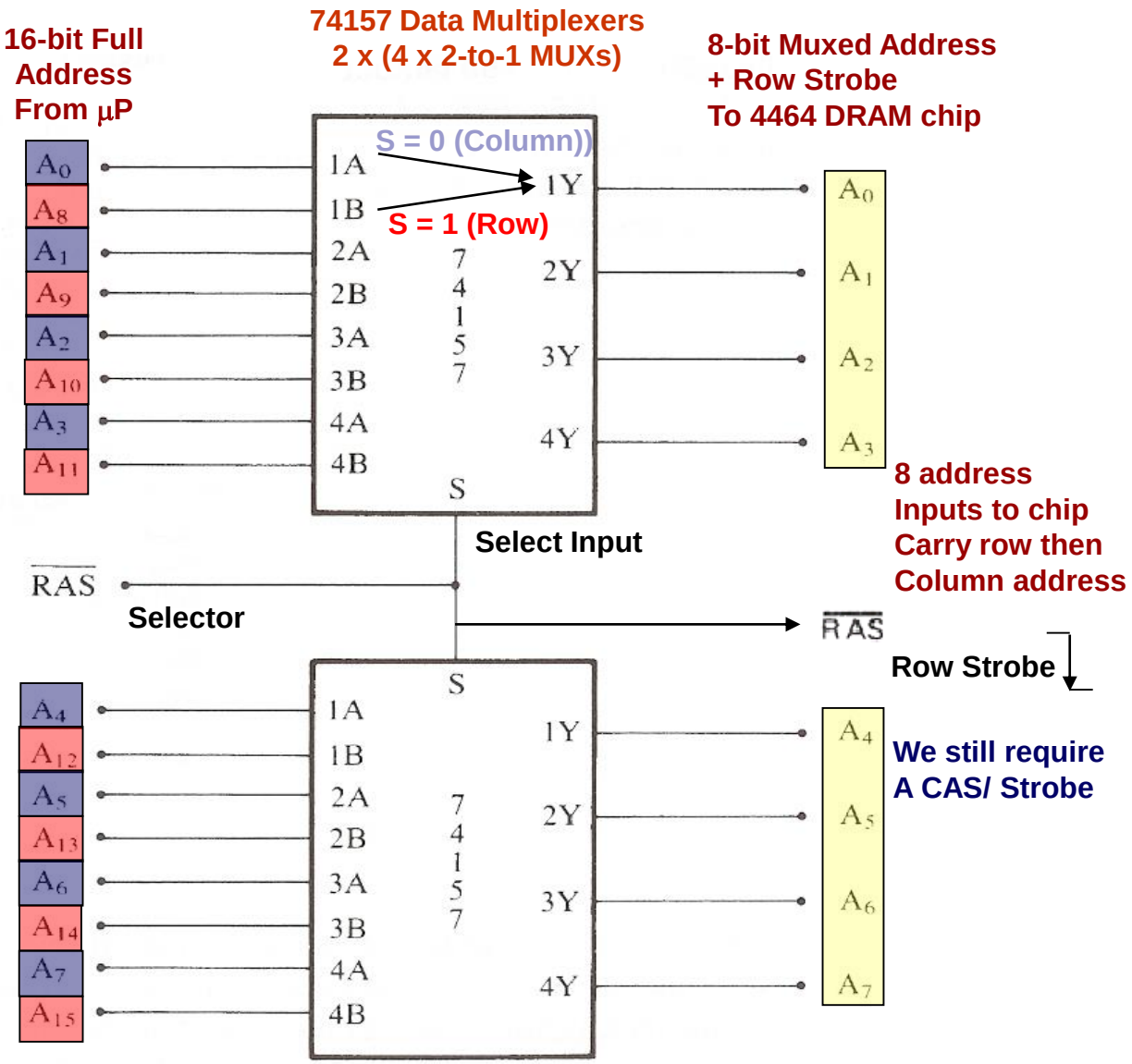
Multiplexing the Row/Column Address

A0-A7: 8-bit Column Address (LS)

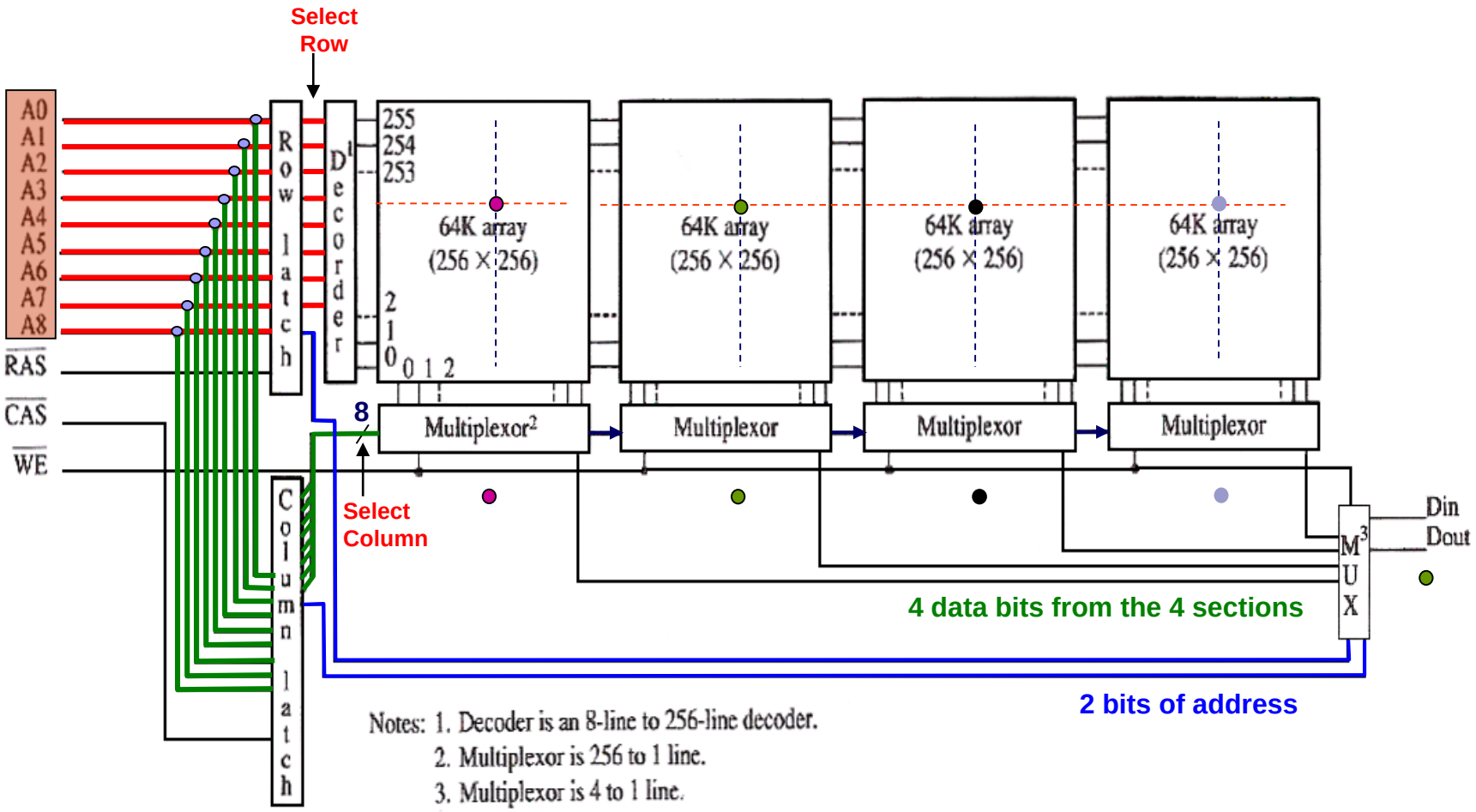
A8-A15: 8-bit Row Address (MS)



- MUX delay > Required Hold time for row address
- RAS/ can be used as a selector I/P for the MUX and also as input to the DRAM to strobe row address in.
- RAS/ signal select the row then the Column address & its falling edge strobes in the row address



Internal Structure of a DRAM

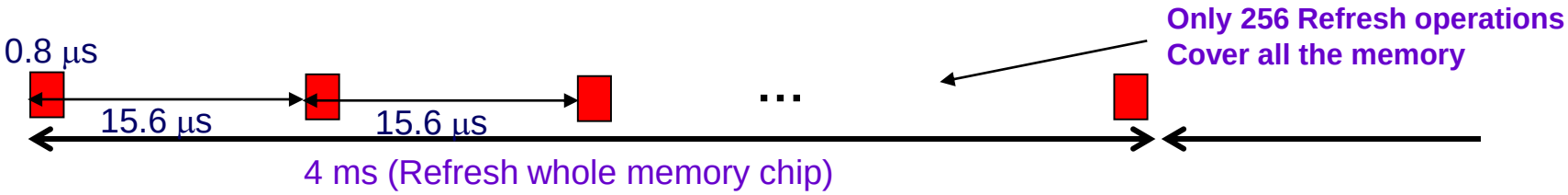


Internal Structure of a DRAM

- 4 sections of 256 x 256 bits each
- Each section is addressed by 8 bits of rows and 8 bits for columns
- Remaining 2 address bits select the section addressed
- Row and column addresses are common to all 4 sections
- A whole row of 4 x 256 = 1024 bits is addressed simultaneously (Speeds up refreshing)
- The 4 data bits in the addressed column in the 4 sections are addressed simultaneously
- Only the bit from the required section is selected by the remaining 2 address bits using MUX3

DRAM Memory Refreshing

- When a row is accessed in a refresh cycle, all memory cells on that row are refreshed
- This means that we need only 256 refresh operations to refresh all the 256K x 1 DRAM above
- To refresh the whole memory at the minimum rate of once every 4 ms, we need to do a refresh cycle every **4 ms/256 = 15.6 ms**



- If a refresh cycle needs a bus cycle (4T with the 8088/86), the % of bus cycles lost for refreshing an 8088/86 running at a clock speed of 5 MHz is:

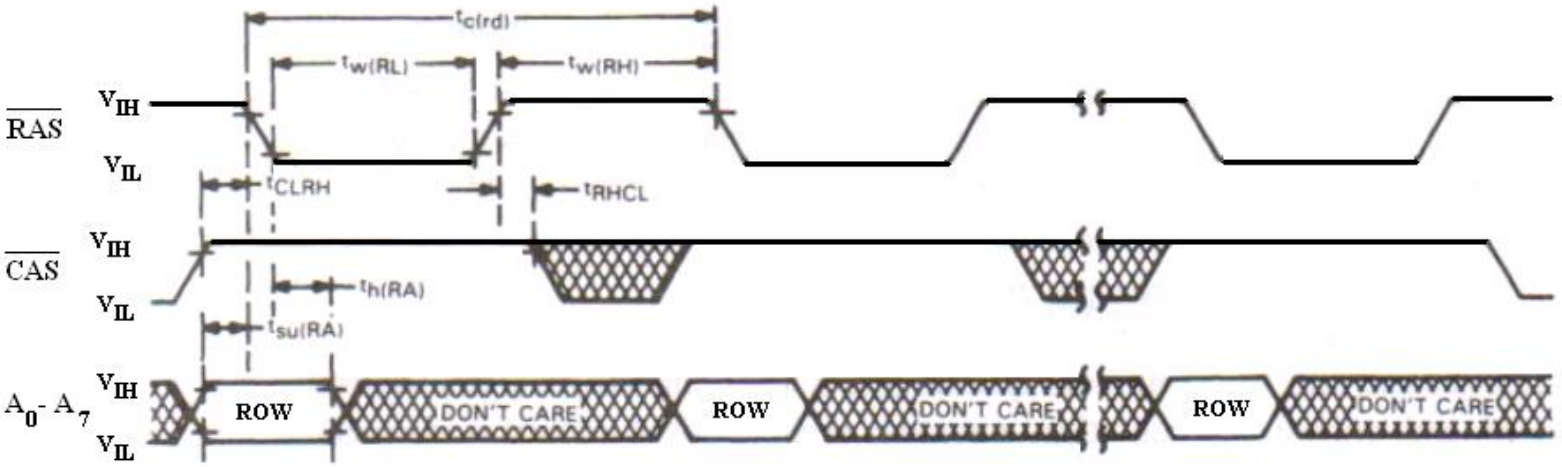
  = 4 x 0.2 ms / 15.6 ms = 5.1% (not bad … for the cost saving we achieve using dynamic RAM)

- For a Pentium 4 with a clock cycle of 3 GHz and a bus/instruction cycle of 1T, this % is:

  = 1 x 0.33 ns / 15.6 ms = 0.2% (i.e. the penalty for DRAM refreshing is much more tolerable with modern, faster processors)

Refresh Cycle

- RAS/ only refresh cycles



The timing Diagram of the RAS/ refresh cycle for the TMS4464 DRAM

- RAS/ strobes a row address indicating the row of bits to be accessed for refreshing
- This row address is not a full memory address and can be generated by a **small on-chip counter** (e.g. 8-bits for the 256 rows in the 256K x 1 DRAM described)
- The row cells read are fed back for re-writing into the same locations to fulfill refresh requirements

Internal Structure of a DRAM

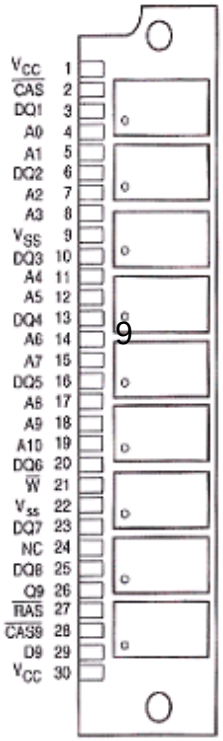
- **EDO (Extended Data Output) Memory**
  - All 256 bits of the row from the selected section are saved in latches on the memory chip. So this data will be ready for future access without experiencing the slow memory access time again
  - Such locations are close to the already accessed data, and are likely to be accessed soon (locality principle)
  - Improves system performance by 15-25%
- **SDRAM (Synchronous Dynamic RAM) Memory**
  - Memory runs synchronously to the system bus clock, e.g. at 100-133-200 MHz
- **Burst (block) Transfers**
  - Burst transfers of say 4 x 64-bit numbers between the processor and the memory. First number experiences normal wait states, but 2^{nd}, 3^{rd}, and 4^{th} transfers suffer no wait states, thus improving average access time.
- **DDR (Double Data Rate) Memory**
  - Data Transferred at double the SDRAM rate by using the two edges of the clock
  - This does not exactly double the data transfer rate due to access time limitations
- **Combinations exist, e.g. DDR SDRAM**

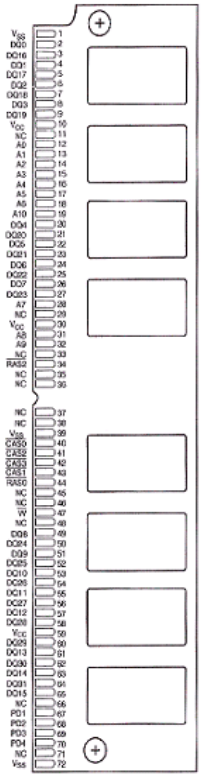
DRAM Memory Modules

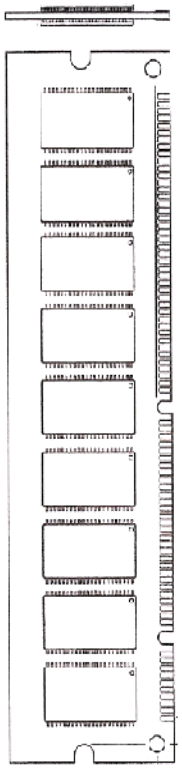
- DRAMs are often mounted on memory modules interfaced to the PC
- **SIMM:** Single In-Line Memory Module: Devices and connection pins mounted on one side. Available in 2 types:
  - Older 30-Pin SIMMs
  - Newer 72-Pin SIMMs
- **DIMM:** Dual In-Line Memory Module: Devices and pins mounted on both sides. 168-Pin

  Used for Pentium- Pentium 4 processors with 64-bit data bus (8 Bytes of data for each memory address)

  Card can have one EPROM containing info on size and speed of the devices for Plug-and-Play use







30-Pin SIMM
(1 Byte)
4 M x 9 bits
= 4M x (8 + 1 Parity)
= 4MB of data

72-Pin SIMM
(4 Bytes)
4 M x 36 bits
= 4M x (32 + 4 Parity)
= 16 MB of data

- Larger address
- Wider data bus

168-Pin DIMM
(8 Bytes)
4 M x 64 bits
= 32 MB of data

In DRAM, EDO, and SDRAM