EE 312

Fundamentals of Electronics LAB

LAB Manual

PART I

Turki Almadhi,

Lecturer, EE Dept.

Version

4.9

21/05/39

Course Policy

OBJECTIVES

To introduce the students to the basic electronic devices and their applications as well as building their circuit construction and design skills.

EVALUATION AND GRADING POLICY

Performance (including attendance)	10%
Homework	5%
Reports / Presentations	20%
Midterm	25%
Final	40%

LAB MANUAL: http://fac.ksu.edu.sa/talmadhi/course/157758

Instructor	Turki Almadhi	Ghazi Isaac
E-mail	talmadhi@ksu.edu.sa	ghazi@ksu.edu.sa
URL	fac.ksu.edu.sa/talmadhi	faculty.ksu.edu.sa/54622/default.aspx
Office	2C 11	AB 92

Course Schedule

Week No.	Activity	notes
2	Experiment 1	
3	Experiment 2	
4	Experiment 3	Submit Report 1 (Exp. 1 + Exp. 2)
5	Experiment 4	
6	Experiment 5	*Go to AC 123* Submit HW1, HW2, HW3, HW4
7	**Midterm Exam**	Submit Report 2 (Exp. 3 + Exp. 4+Exp. 5)
8	Experiment 6	
9	Experiment 7	
10	Experiment 8	Submit Report 3 (Exp. 7 + Exp. 8)
11	Experiment 9	
12	Experiment 10	
13	Revision	Submit HW5, HW6, HW7, HW8, HW9, HW10
14	**Final Exam**	Submit Report 4 (Exp. 9 + Exp. 10)

EXPERIMENT

1

Exploring and Testing Junction Diodes

OBJECTIVES:

- To identify the common types of junction diodes.
- To learn and apply a technique or two to test junction diodes using a multi-meter.
- To explore the basic principle of operation of junction diodes using a simple circuit.

MATERIALS:

- Laboratory setup, including rastered socket panel
- 2 silicon diodes (e.g., the 1N4001 rectifier diode)
- 1 germanium (Ge) diode
- 1 light emitting diode (LED)
- 1 Zener diode (e.g., 1N4733A)
- 1 resistor (1 kΩ)
- Several wires and bridging plugs

INTRODUCTION

A p-n junction diode is a two-terminal electronic device which has important applications that we shall explore in this lab. The p-side of the junction is called the ***anode*** while the n-side is called the ***cathode*** (Fig. 1a). The diode is characterized by a low resistance to current flow in the forward direction (into the anode and out of the cathode), and very high resistance in the reverse direction.

In dc circuits, a forward-biased diode can be approximately modeled by a constant voltage that depends on its type and characteristics. On the other hand, a reverse-biased diode can be modeled by an open circuit.

In this experiment, four types of diodes –the ordinary silicon diode, the germanium diode, the Zener diode and the light emitting diode (LED)– are introduced. A Zener diode is a special type of a silicon diode that is designed and manufactured to operate safely in the reverse breakdown region. An LED is a special type of diode that converts a forward current in light.

Diodes for high-power applications which draw lots of current or rectify high voltages are given the name **rectifier diodes**. On the other hand, diodes that are designed to have high switching speeds go by names such as *signal*, *fast recovery* or **switching diodes** [9].

The *cathode* of a diode is usually marked by a band or a dot. It also can be identified based on a simple test using a digital multimeter (DMM). To test a diode by a DMM, connect the diode between the V **Ω** (red) and the COM (black) jacks of the DMM:

- If an “OL” (open circuit) response does not change upon connecting the diode ⇒ the diode is reverse-biased and acting as an open circuit–in this case, its *cathode* is the lead connected to the V **Ω** (*red*) jack of the DMM.
- If, on the other hand, the DMM displays a voltage drop upon testing the diode ⇒ the diode is forward-biased and its *cathode* is connected to the COM (*black*) jack (see Fig. 1.1b).
- If the DMM displays an “OL” or some low voltage drop in ***both*** directions upon testing a diode ⇒ the diode is defective.

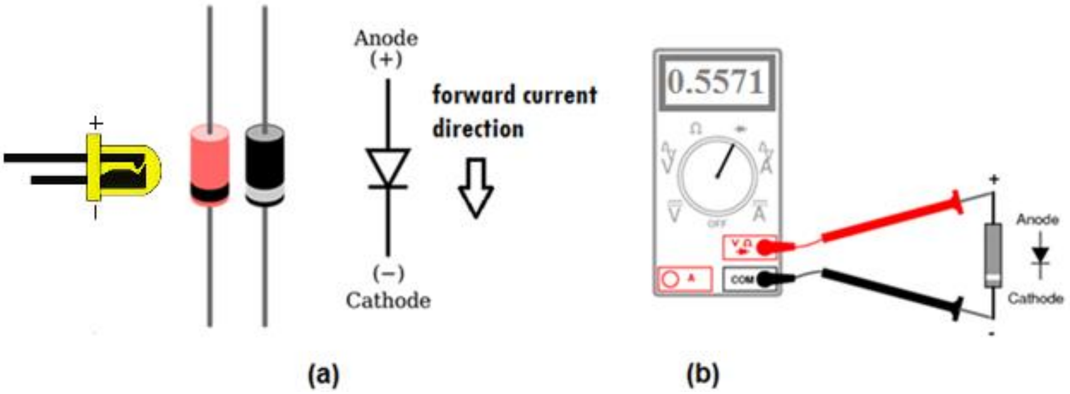


FIGURE 1.1 (a) Diode shape and symbol. **(b)** Testing a diode using a DMM.

PROCEDURE

1. Set your DMM to diode-test mode.
2. Observe and record the open-circuit reading of the DMM in Table 1.1.
3. Connect any type of diode between the V (red) input jack and the COM (black) input jack of the DMM (Fig. 1.1b).
4. Observe the DMM reading for each type of diode.
5. Determine the type of diode and identify its cathode based on the approximate expected values given in Table 1.1b. Record your measurements in the table.

6. Connect the circuit shown in Fig. 1.2.
7. Using a dc power supply, apply a 4-V dc voltage to your circuit.
8. Make sure that your digital multimeter is set to measure **dc voltage**.
9. Using a digital multimeter, measure V_{AB} and $V_{1\text{-}k\Omega}$; record their values in Table 1.2.
10. Reverse the diode connection and repeat step 9.
11. Connect two forward-biased silicon diodes between A and B in series then measure V_{AB} and $V_{1\text{-}k\Omega}$.
12. Connect two silicon diodes back-to-back (their anodes connected together) between A and B then measure V_{AB} and $V_{1\text{-}k\Omega}$.
13. Connect a forward-biased LED between A and B then measure V_{AB} and $V_{1\text{-}k\Omega}$.
14. Connect a forward-biased silicon diode in parallel with the LED. *Why does the LED turn off?*
15. Connect a forward-biased germanium diode in parallel with the silicon diode and the LED. *Which diode controls V_{AB} in this case?*

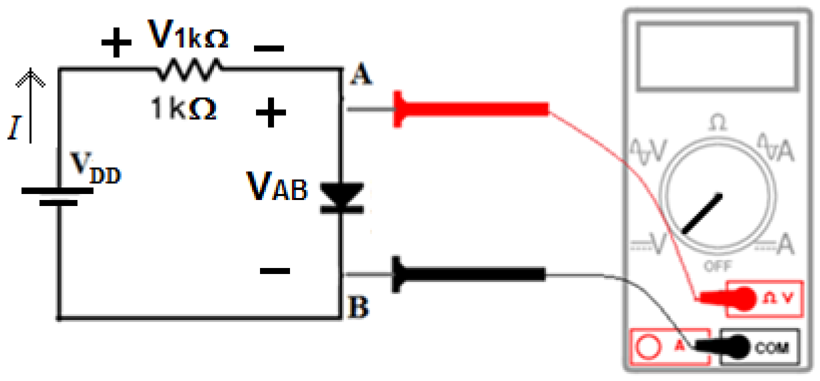


FIGURE 1.2 Exploring the essence of the diode function.

RESULTS

TABLE 1.1 Testing a Diode

DMM Test-Position Reading in Case of an Open Circuit:		
DMM Test-Position Reading in Case of a Reverse-Biased Diode:		
Type of diode	Expected Forward Voltage	Measured Forward Voltage
Si	0.55 ~ 0.75 V	
Ge	0.2 ~ 0.4 V	
Zener	0.55 ~ 0.75V	
LED	1.5 ~ 3.5 V	

TABLE 1.2 Diodes Principle of Operation

Step	Type of Diode	Bias Condition	V_{AB} (V)	$V_{1\text{-}k\Omega}$ (V)	$I = \frac{V_{1-k\Omega}}{1\ k}$
9	silicon	forward			
10	silicon	Reverse			
11	2 silicon diodes in series	forward			
12	2 silicon diodes in series	back to back			
13	LED	forward			
14	LED // Si diode	forward			
15	LED // Si diode//Ge diode	forward			

HOMEWORK

Design an experiment to explore how the dc forward voltage across a diode changes with its cross sectional area if the total dc current is kept constant.

Enlist the required materials and include a circuit diagram and a suggested procedure to conduct the experiment in your answer.

(*Hint: two identical diodes connected in parallel will have double the cross sectional area of a single diode.*)

EXPERIMENT

2

Terminal Characteristics Of Junction Diodes

OBJECTIVES:

- To experimentally obtain the *i-v* characteristic curves for a general purpose junction diode and a Zener diode.
- To get acquainted with Zener diodes and know how they differ from ordinary diodes.
- To be able to extract a piecewise-linear model from an *i-v* characteristic curve.

MATERIALS:

- Laboratory setup, including rastered socket panel
- 1 ordinary silicon diode (e.g., the 1N4001 rectifier diode)
- 1 Zener diode (e.g., 1N4733A)
- 1 resistor (1 kΩ)
- Several wires and bridging plugs

INTRODUCTION

Figure 2.1 shows the $i - v$ relationship of a silicon diode. This relationship consists of three distinct *regions of operation*:

- The forward-bias region ($v > 0$)
- The reverse-bias region ($v < 0$)
- The breakdown region ($v < -V_{ZK}$)

In the forward-bias region, the diode can be represented by an equivalent circuit based on a piecewise-linear model which consists of a **battery** V_{D0} **plus a resistance** r_D.(Fig. 2.2a). The model parameters V_{D0} and r_D can readily be calculated if we know two **operating points (Q-points)** on the forward characteristic. The parameters are not unique for a given diode because they depend on the current range over which they are calculated.

The breakdown region is characterized by a near-vertical line (voltage-source behavior) which is desirable if the diode is to be used in voltage regulation. Diodes specifically manufactured to operate in this region are commonly called **Zener diodes**. Commercial Zener diodes are available having **nominal** Zener voltages of 2.4 to 200 V (in the same standard values as 10% resistances [4]) with power ratings from $\frac{1}{4}$ to 50 W [2].

A Zener diode operating in the breakdown region can be modeled by an **equivalent circuit** based on a piecewise-linear approximation (Fig. 2.2b). The inverse of the slope of the breakdown region characteristic determines the Zener **dynamic resistance** r_Z. Smaller r_Z means steeper characteristic and consequently smaller $\Delta V_Z = \Delta I_Z \times r_Z$, which suggests that we can use a Zener diode in that region as a **voltage reference** or as a **voltage regulator**.

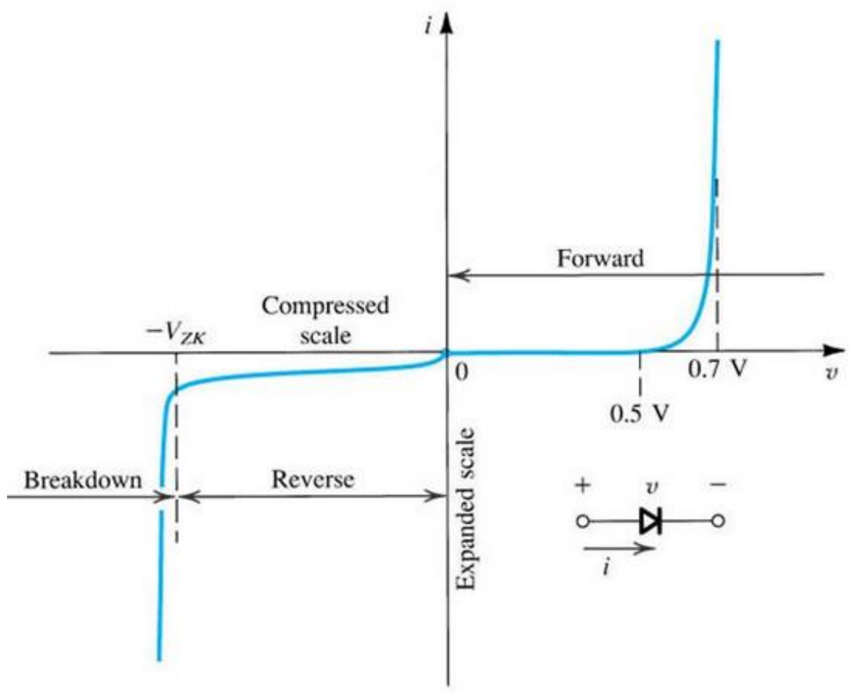


Figure 2.1 The diode i-v characteristic curve [1].

PROCEDURE

1. Using a digital multimeter (DMM), measure and record the actual value of R.

$R =$	kΩ

2. Connect the circuit shown in Fig. 2.3 initially with an ordinary silicon diode.
3. Using a dc power supply, vary the input voltage V_{DD} in steps as shown in Table 2.1.
4. Using a digital multimeter, and for each value of V_{DD}, measure and record V_D and V_R. Calculate the corresponding value of I_D using Ohm's law.

   Note: For the negative values of V_{DD} you will need to swap the dc supply leads on the board. However, the reference polarities for V_R and V_D remain unchanged.

5. Replace the ordinary silicon diode with a Zener diode and complete Table 2.2.

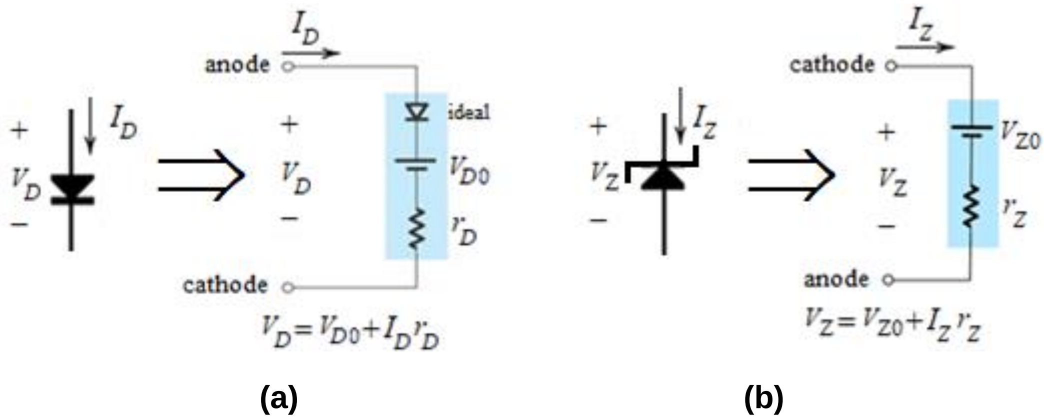


Figure 2.2 Linear model of **(a)** a forward–biased diode, **(b)** a Zener in breakdown.

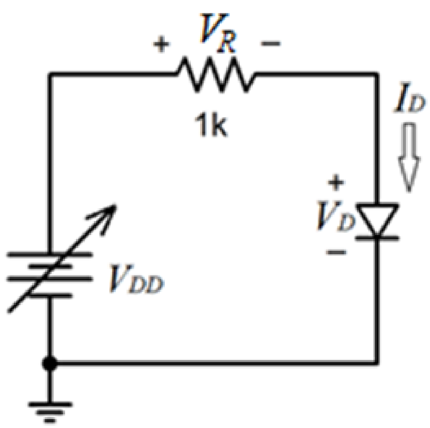


Figure 2.3 Circuit for measuring the i-v characteristics.

RESULTS

Table 2.1 Ordinary Silicon Diode i-v Measured Data

V_{DD} (V)	V_R (V)	V_D (V)	$I_D = V_R/R$ (mA)	V_{DD} (V)	V_R (V)	V_D (V)	$I_D = V_R/R$ (mA)
15				-2			
5				-3			
1.6				-3.5			
0.7				-4			
0.5				-4.5			
0.2				-5			
0	0	0	0	-15			

Table 2.2 Zener Diode i-v Measured Data

V_{DD} (V)	V_R (V)	V_D (V)	$I_D = V_R/R$ (mA)	V_{DD} (V)	V_R (V)	V_{DZ} (V)	$I_{DZ} = V_R/R$ (mA)
15				-2			
5				-3			
1.6				-3.5			
0.7				-4			
0.5				-4.5			
0.2				-5			
0	0	0	0	-15			

HOMEWORK

1. Plot I_D vs. V_D for both diodes using MATLAB® (see Appendix A). Label the three regions of operation.
   You have to print and attach the code as well as the graph with your name in the subtitle.
2. Extract a piecewise-linear model for the silicon diode in the forward region (Fig. 2.3a) using (V_{D1}, I_{D1}) that you have measured at V_{DD} = 1.6 V and (V_{D2}, I_{D2}) that you have measured at V_{DD} = 15 V. This can easily be done as follows:

   i. Calculate r_D given that $r_D = \frac{1}{Slope} = \frac{\Delta V_D}{\Delta I_D} = \frac{V_{D2}-V_{D1}}{I_{D2}-I_{D1}}$

   ii. Calculate V_{D0} given that

   $V_{D1} = V_{D0} + I_{D1} \times r_D$ and $V_{D2} = V_{D0} + I_{D2} \times r_D$

3. For V_{DD} = 5 V, use the piecewise-linear model you have obtained above to calculate I_D and V_D.
4. Calculate the error % in the V_D obtained in (3) with respect to the measured value that you have recorded in Table 2.1 Tabulate your results as shown below.

Method	V_D (V)	I_D (mA)	V_D error %	I_D error %
Measured (from Table 2.1)			0	0
Using the piecewise-linear model approximation				

5. Extract a piecewise-linear model for the Zener diode in the reverse breakdown region (Fig.2.3b) using ($|V_{D1}|$, $|I_{D1}|$) that you have measured at V_{DD} = -5 V and ($|V_{D2}|$, $|I_{D2}|$) that you have measured at V_{DD} = -15 V. This can easily be done as follows:

   i. Calculate r_Z given that $r_Z = \frac{1}{Slope} = \frac{\Delta V_D}{\Delta I_D}$ (in the breakdown region)

   ii. Calculate V_{Z0} given that
   $V_{Z1} = |V_{D1}| = V_{Z0} + |I_{D1}| \times r_Z$ and $V_{Z2} = |V_{D2}| = V_{Z0} + |I_{D2}| \times r_Z$

EXPERIMENT

3

Limiting Circuits

OBJECTIVES:

- To explore the basic principles of some limiting (clipping) circuits and be able to predict their responses.
- To experimentally obtain and examine the output waveforms and the voltage transfer characteristics of some typical circuits of that type.
- To be able to design and implement a circuit to satisfy a given limiting transfer characteristic.

MATERIALS:

- Laboratory setup, including rastered socket panel
- 2 silicon diodes (e.g., the 1N4001 rectifier diode)
- 2 Zener diode (e.g., 1N4733A)
- 1 resistor (1 kΩ)
- Several wires and bridging plugs

BACKGROUND

Limiting or clipping is a function performed by a diode network if prevention of the output voltage from exceeding or falling below a predetermined voltage level is desired. A diode is suitable for this role because its voltage changes a little for a significant change in its current.

Fig. 3.1 shows the general voltage transfer characteristic (VTC) for a double limiter. The circuit operation can be divided into two regions:

- linear, where $(V_O^-/A_V) < v_I < (V_O^+/A_V)$, and
- saturation which extends outside that range.

If there is no load connected across its output port, a limiter will have a unity slope in the linear region of its VTC; i.e., $A_V = 1$, and the threshold levels will be equal to the limiting levels. In that case:

- If $V_O^- < v_I(t) < V_O^+ \Rightarrow v_O(t) = v_I(t)$.
- If $v_I(t)$ exceeds the upper *threshold* $(V_O^+/A_V) = V_O^+$, the output voltage is clamped or *limited* to the upper limiting level V_O^+. If, on the other hand, $v_I(t)$ is reduced below the lower threshold, $v_O(t)$ is limited to the lower limiting level V_O^-.

The limiting levels of a given limiting circuit can designed to meet a given specification. Toward that end, the diode forward drop and/or the Zener voltage V_Z can be utilized to obtain certain limiting levels of a desired transfer characteristic.

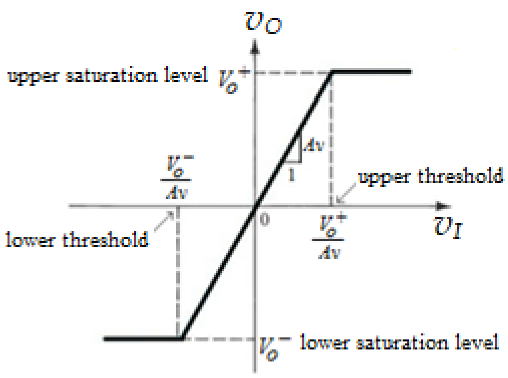


Figure 3.1 General transfer characteristic for a double limiter circuit.

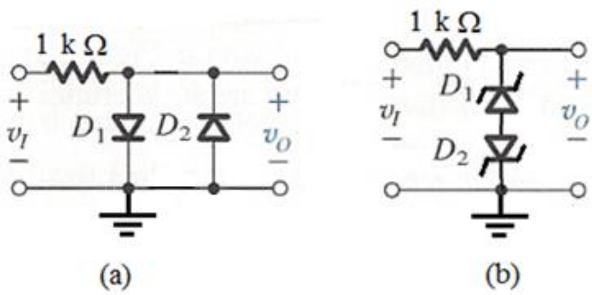


Figure 3.2 **(a)** The antiparallel diode double limiter. **(b)** The double-anode Zener limiter.

PROCEDURE

1. Assemble the circuit shown in Fig. 3.2a.
2. Using a function generator, apply to its input port a 100-Hz, 6-$V_{pk\text{-}pk}$ sinusoid with no dc component.
3. Using an oscilloscope, display v_I(t) on CH1 (**X**) and v_O(t) on CH2 (**Y**).
   Use appropriate vertical and horizontal sensitivities and take note of them. Also, use dc coupling on both channels of your scope.
4. Sketch v_I(t) and v_O(t) on Fig. 3.3a.
5. Record what you observe when D_2 is disconnected.
6. Reconnect D_2. Set your scope on X-Y mode. Set both channels to GND. Adjust the position of the dot-shaped beam to align it at the origin. Set both cannels to dc coupling again.
7. Sketch the displayed voltage transfer characteristics of your circuit on Fig. 3.3b.
   What is the upper limiting (saturation) level of the output? What is the upper threshold of the input?

8. Connect the circuit shown in Fig. 3.2b.
9. Using a function generator, apply to its input port a 100-Hz, 14-$V_{pk\text{-}pk}$ sinusoid with no dc component.
10. Sketch v_I(t) and v_O(t) on Fig. 3.4a.
11. Go back to the X-Y mode of your scope to display the VTC of your circuit.
12. Sketch the displayed voltage transfer characteristics of your circuit on Fig. 3.4b
    Determine the upper limiting (saturation) level of the output; i.e., V_O^+.
    Assuming a 0.7-V forward drop, what is the expected value of V_O^+ in terms of V_Z?
    Calculate V_Z.

RESULTS

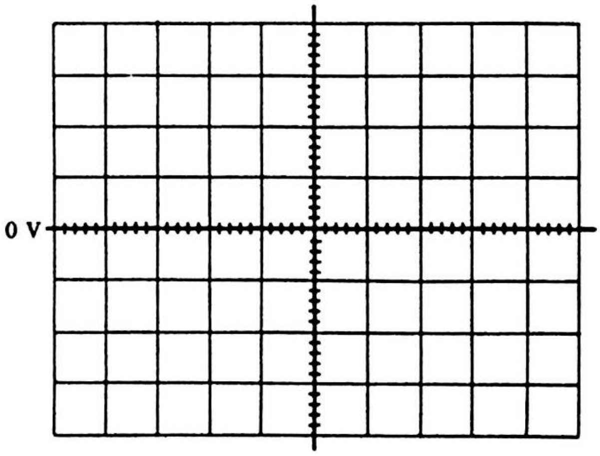


Figure 3.3a

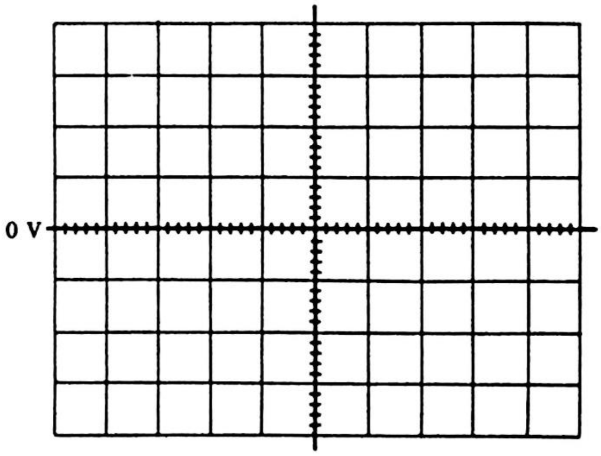


Figure 3.3b

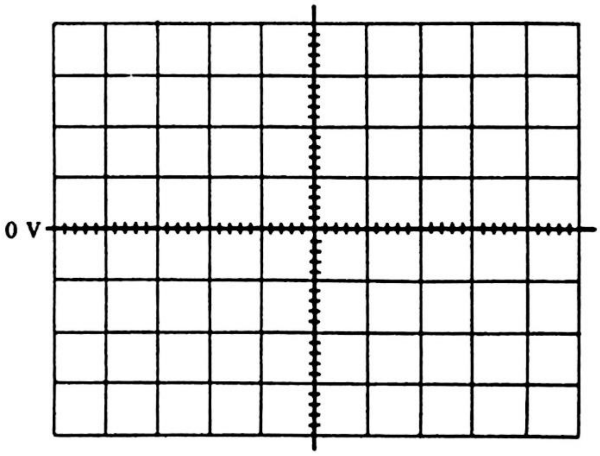


Figure 3.4a

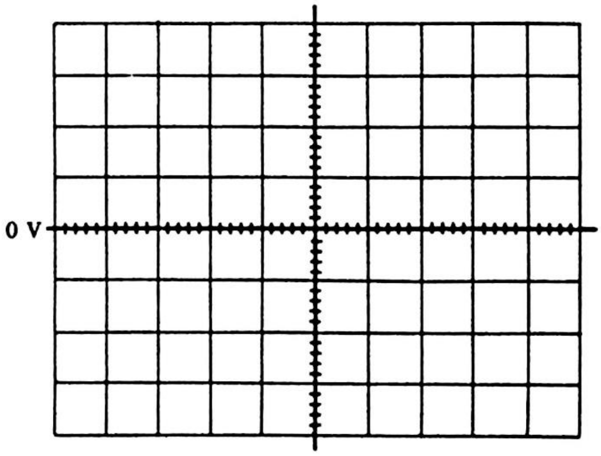


Figure 3.4b

HOMEWORK

1. Design a circuit that implements the transfer characteristic shown in Fig. 3.5a.
   Assume a 0.6-V forward drop model for an ordinary silicon diode.
2. Sketch the *expected* transfer characteristic for the circuit shown in Fig. 3.5b
3. A 20-$V_{pk\text{-}pk}$ sinusoid is applied to the input of the circuit shown in Fig. 3.5b. Sketch the *expected* output voltage waveform $v_O(t)$.
   For a Zener diode, use a 0.7-V forward drop and a constant-voltage-drop model of V_Z in the breakdown region. Use the same V_Z that you have obtained in this experiment.
4. Repeat the above question in case of a 5-$V_{pk\text{-}pk}$ sinusoidal input.

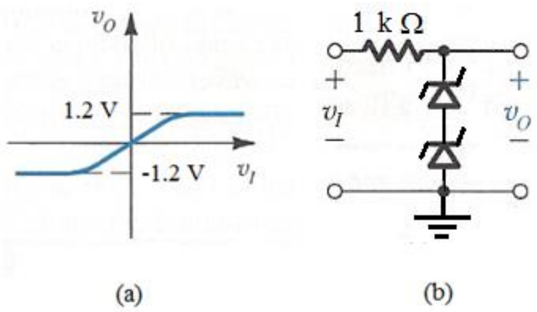


FIGURE 3.5

EXPERIMENT

4

Rectifiers

OBJECTIVES:

- To introduce the student to an important application of diodes, namely the rectifier
- To emphasize the importance of filtering and voltage regulation in the process of ac to dc conversion.
- To apply some practical design tips for designing full-wave rectifier circuits.

MATERIALS:

- Laboratory setup, including rastered socket panel
- 1 center-tapped transformer
- 2 silicon diodes (Si) (e.g., the 1N4001 rectifier diode)
- 2 electrolytic capacitors (10 μF, 470 μF)
- 1 resistor (1 kΩ)
- Several wires and bridging plugs

INTRODUCTION

Electronic equipment needs dc power supply to operate. A block diagram of such a system is shown in Fig. 4.1 [1]. This system involves rectification, filtering and voltage regulation.

A **power transformer** is used to step down the input ac voltage and provide electrical isolation (important for safety). A **diode rectifier** uses the unidirectional-current property of diodes to convert an input sinusoid to a unipolar but pulsating output. Acting as a simple low-pass filter, a capacitor is used to reduce the pulsation (**ripple**) of the resulting output waveform.

However, the ripple would be inversely proportional to C and R_L. So, a **voltage regulator** is needed to regulate the dc output voltage against load and/or ac input variations. We shall examine the effect and benefits of voltage regulation in experiment 5.

There are two main implementations of a full-wave rectifier: the one that utilizes a **center-tapped** transformer and requires only two diodes (see Fig. 4.2b) and the **bridge rectifier** that does not require a center-tapped transformer but requires four diodes. We shall explore the bridge rectifier in experiment 5. The output voltage ripple peak-to-peak V_r is related

Two important parameters are needed to be specified when an engineer needs to select diodes for a given rectifier design: the **p**eak **i**nverse **v**oltage (**PIV**) and current-handling capability. The PIV is the maximum reverse voltage that the diode ever experiences in a given circuit [4].

A manufacturer's data sheet gives detailed information on a device so that it can be used properly in a given application. Appendix C shows the data sheet for general-purpose rectifier diodes (1N4001 – 1N4007). $\mathbf{V_{RRM}}$ is the maximum peak repetitive reverse voltage that can be applied across the diode. $\mathbf{I_{F(avg)}}$ is the maximum average rectified forward current at T_A=75°C. $\mathbf{I_{FSM}}$ is the maximum forward **surge** current the diode can sustain.

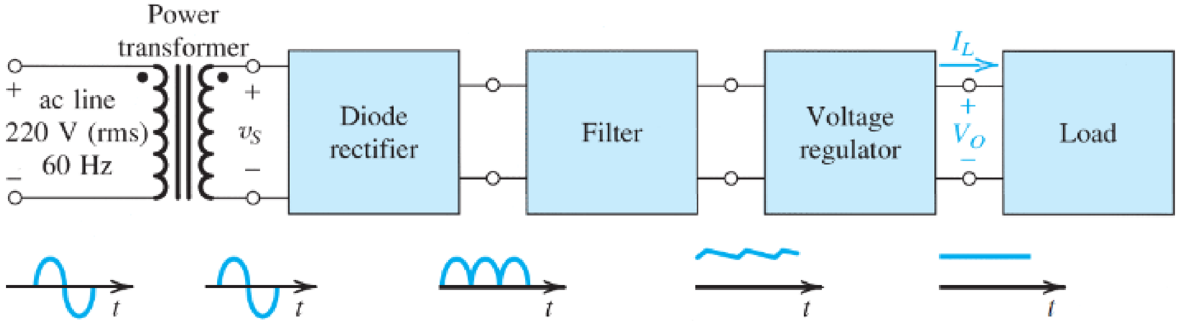


Figure 4.1 A block diagram of a dc power supply [1].

DESIGN TIPS

Use the following checklist to complete a full-wave rectifier design given the frequency *f*, the value of the load resistance R_L, the secondary peak voltage V_s of the transformer and the output voltage ripple peak-to-peak V_r .

1. Determine the dc component of the load current I_L using the following equation:
$$I_L = \frac{V_s - 0.5V_r}{R_L} \tag{4.1}$$
2. Determine C using the following equation:
$$C = \frac{1}{2f} \times \frac{I_L}{V_r} = \frac{1}{120} \times \frac{I_L}{V_r} \tag{4.2}$$
3. Select a standard value of C from the table given in Appendix E.
4. Determine the diode average forward current using the following equation:
$$i_{Dav} = I_L(1 + \pi\sqrt{\frac{V_s}{V_r}}) \tag{4.3}$$
5. Determine the PIV rating for the diodes you are going to need, this will depend on the type of rectifier circuit you plan to build.
6. Determine the $\mathbf{V_{RRM}}$ rating of the diodes based on the PIV. A good practice is to have $\mathbf{V_{RRM}}$ = 1.5 PIV
7. Determine the $\mathbf{I_{F(avg)}}$ rating of the diodes based on i_{Dav}. A good practice is to have $\mathbf{I_{F(avg)}}$ = 1.5 i_{Dav}
8. Look for a rectifier diode that has at least the same ratings as determined in the above two steps.
9. Knowing $\mathbf{I_{FSM}}$ of the diode you have picked, determine R_{surge} needed to limit the diode surge current based on the following equation:
$$R_{surge} = \frac{V_S}{0.8 \times \mathbf{I_{FSM}}} \tag{4.4}$$
10. Select a standard value of R_{surge} from the table given in Appendix E.

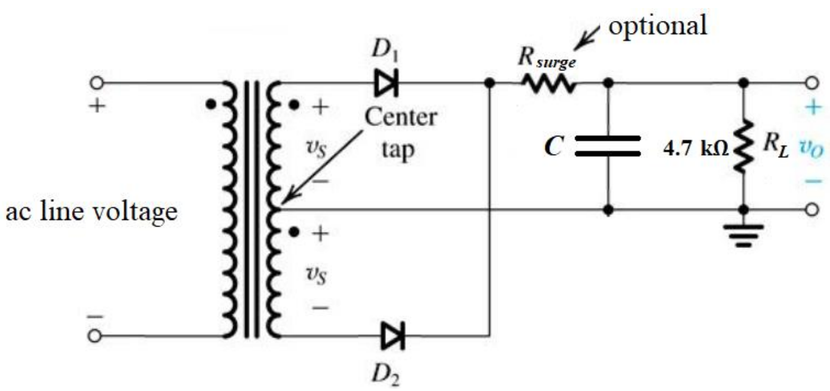


Figure 4.2 Rectifier using a center-tapped transformer.

PROCEDURE

The Half-Wave Rectifier:

1. Connect the circuit shown in Fig. 4.2 initially without D_2.
2. Using an oscilloscope, display v_S(t) on channel I (**X**) and v_O(t) on channel II (**Y**).
3. Set both channels of your oscilloscope to *setting 1* (Table 4.1).
4. Display both waveforms at the same time by setting the scope on DUAL display mode.
5. Record v_S(t) and v_O(t) on Fig. 4.3.
6. using a digital multimeter set to measure dc volts, measure and record the average value of v_O(t).

The Full-Wave Rectifier:

7. Connect D_2 then record v_S(t) and v_O(t) on Fig. 4.4.
8. Using a digital multimeter, measure and record the average value of v_O(t).

The Effect of Filtering:

9. Set channel 2 of your scope to *setting 2* (Table 4.1). Connect a 10-µF electrolytic capacitor (with its negatively marked lead connected to ground) in parallel with R_L.
10. Record v_O(t) on Fig. 4.5.
11. Replace the 10-µF capacitor with a 470-µF one.
12. Record v_O(t) on Fig. 4.6.

The Effect of Reducing R_L:

13. Replace the 4.7-kΩ resistor with a 270-Ω one. Observe how the ripple changes if R_L is reduced.

TABLE 4.1 Oscilloscope settings

Setting	Vertical Sensitivity VOLT/DIV	Horizontal Sensitivity mS/DIV	Coupling	Ground Level Position	Trigger
1	5	5	dc	center	Line (ac)
2	2	5	dc	bottom	Line (ac)

RESULTS

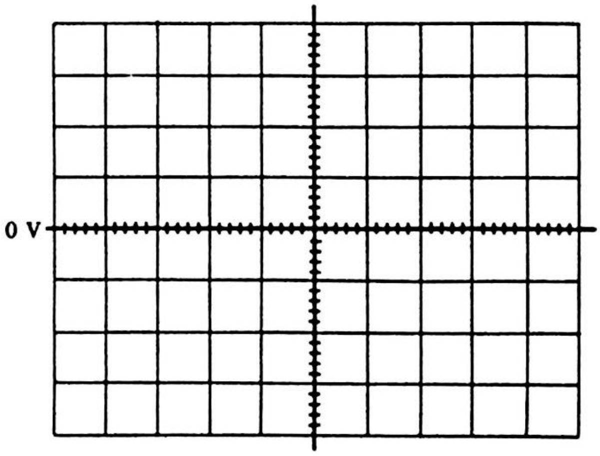


Figure 3.3

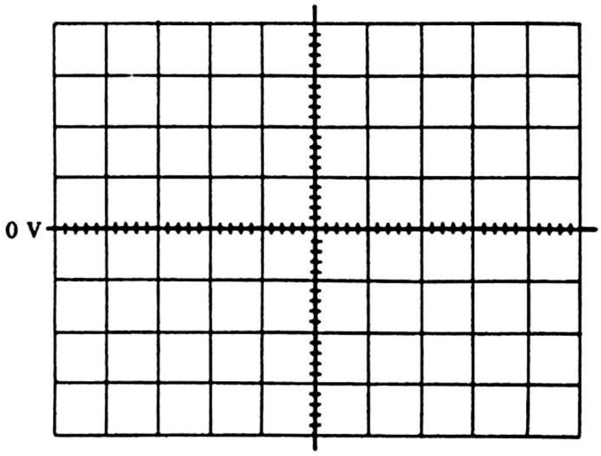


Figure 3.4

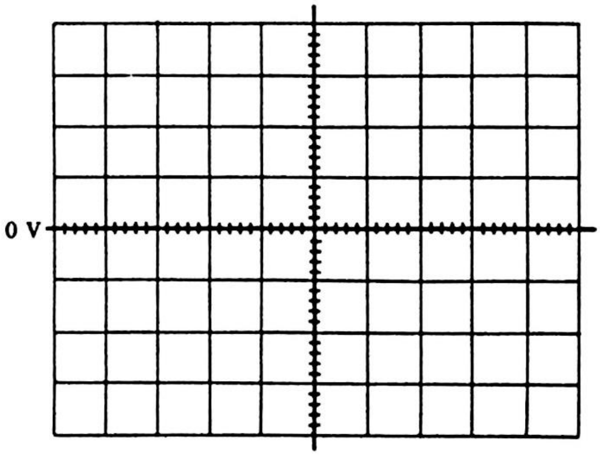


Figure 3.5

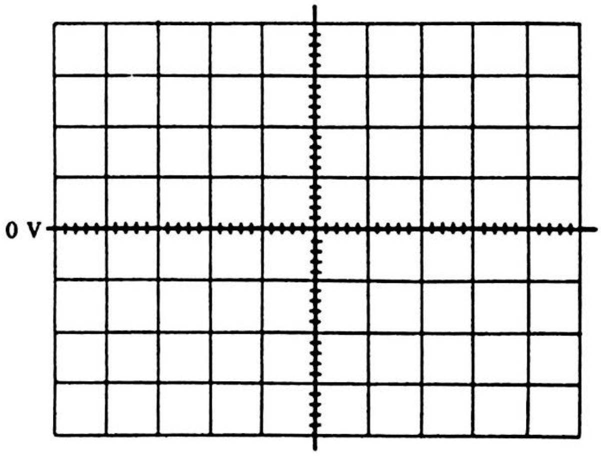


Figure 3.6

HOMEWORK

Using the steps given on the design tips section, design a full-wave rectifier with a filter capacitor to supply a dc load of I_L = 200 mA. Assume V_s of 10 V is available from each of the secondary windings of a center-tapped transformer. The maximum ripple to be tolerated is V_r = 1 $V_{pk\text{-}pk}$. Look on the internet or Appendix C for a rectifier diode that can be used for your design.

EXPERIMENT

5

Computer Simulation of Electronic Circuits

OBJECTIVES:

- To learn how to simulate electronic circuits using freely available on the internet design tools like the OrCAD (Capture & PSpice) software.
- To see why a voltage regulator is needed in ac to dc conversion systems with the aid of simulation.

MATERIALS:

- A PC or a laptop with a Lite Demo version of OrCAD (Capture & PSpice) installed

INTRODUCTION

OrCAD (Capture & PSpice) is a version of SPICE (Simulation Program for Integrated Circuit Engineering). SPICE was developed at the University of California at Berkeley in the 1970s, and has been the most widely used circuit simulator in the electronics industry. The required steps to using OrCAD (Capture & PSpice) can be summarized as follows:

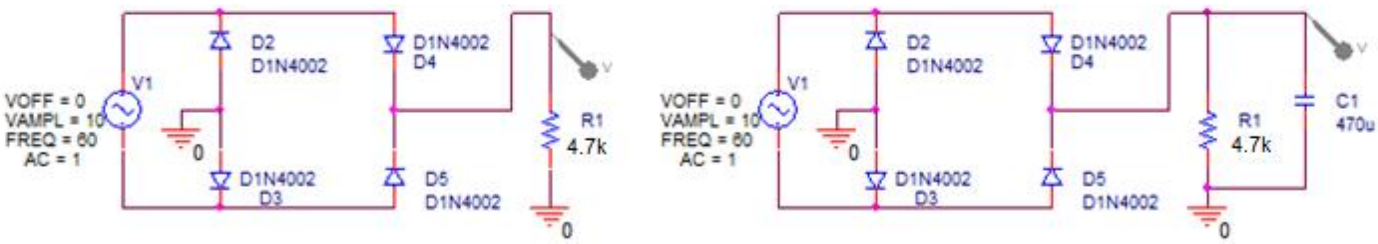
1. Draw an electronic circuit on the computer using Capture.
2. Setting an appropriate simulation profile that includes analysis types like: bias point, dc sweep, ac sweep and time domain.
3. Running PSpice from within Capture to obtain the results/plots of the chosen analysis in step 2.

A good introduction to OrCAD (Capture & PSpice) can be found here:

http://userweb.eng.gla.ac.uk/john.davies/orcad/spiceintro160.pdf

The latest version of the OrCAD Lite Demo software (Capture & PSpice) can be downloaded via the following link:

http://www.orcad.com/resources/orcad-downloads



(a) **(b)**

Figure 5.1 Bridge rectifier **(a)** without filtering and **(b)** with filtering.

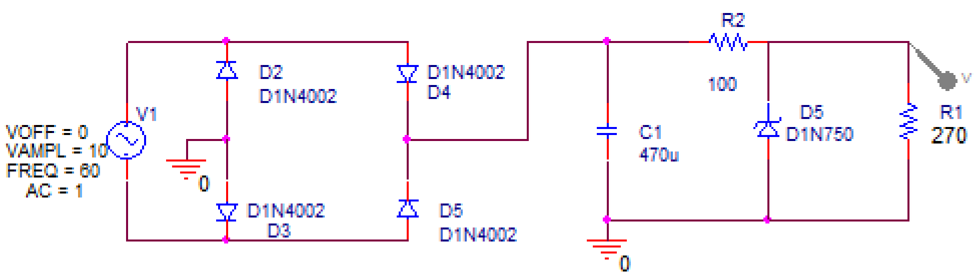


Figure 5.2 Regulated power supply.

PROCEDURE

1. Double click the OrCAD Capture icon on the desktop.
2. Go to File ⇨ New Project. Your project should be named: ckt2_xxxx, where xxxx stands for the last four digits of your student number. Keep the first choice selected. In the second window select: Create a blank project then click OK.
3. First, you have to add all of the needed parts on the work area. You may do that either by clicking on the ***Place part*** icon on the right-hand toolbar or simply typing **p**. The parts to be added are: VSIN/SOURCE, R/ANALOG, D1N4002/EVAL (4),
4. Wire all the parts as shown in Fig. 5.1a. You may do that either by clicking on the ***Place wire*** icon on the right-hand toolbar or simply typing **w**.
5. Ground your circuit where it is needed. You may do that either by clicking on the ***Place ground*** icon on the right-hand toolbar or simply typing **g**; use the 0/CAPSYM type of ground.
6. Double click on each V1 parameter and set it at the value shown in Fig. 5.1a.
7. From PSpice (top menu), select: New Simulation Profile. Name it for example: dc_sweep. Set analysis type at: dc Sweep. Set the sweep variable to V_1. Start from -10 and end at 10 with an increment of [10-(-10)]/1000 = 20m.
8. Place a voltage/level marker on top of the R_1 to display the transfer characteristic of the circuit.
9. Run your simulation and examine characteristic. What mathematical function does it look like?
10. From PSpice (top menu), select: New Simulation Profile. Name it for example: time_domain. Set analysis type at: Time Domain (transient). Start from 0 up to 50ms (3 cycles of our 60-Hz input) with a maximum step size of 50ms/1000 = 50us.
11. Place a <u>**differential voltage marker**</u> across the input.
12. Run your simulation and examine the input and output voltage waveforms. *Does the output waveform look familiar to you? What does this circuit do?*
13. Connect the capacitor as shown in Fig. 5.1b and rerun the simulation to see how that affects the ripple in the output voltage waveform.
14. Decease the value of R_1 to 270 **Ω** and rerun to see how that affects the ripple in the output.
15. Add a voltage regulator to your dc supply circuit as shown in Fig. 5.2. Change R_1 back to 4.7 kΩ. Rerun the simulation. *What does the output waveform look like? How is the output voltage level related to V_Z of the Zener diode?*
16. Reduce R_1 to 270 **Ω** and rerun to see how that affects the ripple in the output.

What is your conclusion about the importance of the voltage regulator?

HOMEWORK

1. Using an appropriate number of D1N4002 diodes, simulate the circuit you designed in the homework of experiment 3 (page 18).
2. Double click the OrCAD Capture icon on the desktop.
3. Go to File ⇨ New Project. Your project should be named: ckt2_xxxx, where xxxx stands for the last four digits of your student number. Keep the first choice selected. In the second window select: create a blank project then click OK.
4. Draw the circuit that you have designed in homework 3.
5. For the input source V_1, use a (VSIN) part with 4-V peak amplitudeude, 1-kHz frequency and a zero offset.
6. From PSpice (top menu), select: New Simulation Profile. Name it for example: time_domain. Set analysis type at: Time Domain. Start from 0 up to 3 ms with appropriate maximum step size.
7. Place a voltage/level marker on top of V_1 and across the output (on top of D_1).
8. Run your simulation to display $v_i(t)$ and $v_o(t)$.
9. From PSpice (top menu), select: New Simulation Profile. Name it for example: dc_sweep. Set analysis type at dc Sweep. Sweep V_1 from -4 to 4V with appropriate increment.
10. Click on the input voltage/level marker and hit delete on the keyboard.
11. Run your circuit to see its transfer characteristic.
12. Print and submit :
    - The circuit diagram (with your name typed on lower right corner)
    - $v_i(t)$ and $v_o(t)$.
    - The transfer characteristic.
    - From your plots, find the upper and lower saturation levels to verify that they meet the specifications.

Appendix A

MATLAB® Code

(Experiment 2)

```
clf

% store voltage readings for silicon diode below

VD=[                                        ];

% store current readings for silicon diode below

ID=[                                        ];

% store voltage readings for Zener diode below

VDz=[                                       ];

% store current readings for Zener diode below

IDz=[                                       ];

plot(VD,ID,'-dk',VDz,IDz,'-*k')

axis([-6 0.8 -10 12])

grid on

legend('Ordinary silicon diode','Zener diode')

title('The i-v characteristics for a an ordinary silicon diode and a Zener diode', 'put your student no. here')

% Do not forget to type you student number in 'put your student no. here' inside the above title( )
command!!!

xlabel('VD (V)')

ylabel('ID (mA)')
```

MATLAB® Code

(Experiment 7)

```
% plotting ID-VDS characteristics for different values of VGS for NMOS

clf

VDS=[0 0.02 0.05 0.1 0.2 0.5 1 2];

% store current readings for VGS1 below

ID1=[                                      ];

% store current readings for VGS2 below

ID2=[                                      ];

% store current readings for VGS3 below

ID3=[                                      ];

figure(1)

plot(VDS,ID1,'-ob',VDS,ID2,'-dk',VDS,ID3,'-*r')

grid on

legend('VGS1','VGS2','VGS3')

title('The ID-VDS characteristics for NMOS')

xlabel('VDS (V)')

ylabel('ID (mA)')
```

Appendix B

References

[1] A. S. Sedra and K. C.Smith, *Microelectronic Circuits*, New York: Oxford University Press, 2010.

[2] R. Boylestad and L. Nashelesky, *Electronic Devices and Circuit Theory, 7th ed.*, Upper Saddle River, NJ: Prentice-Hall Inc., 1992.

[3] T. Floyd, *Electronic Devices, 7th ed.*, Upper Saddle River, NJ: Pearson Education Inc., 2005.

[4] S. Franco, *Analog Circuit Design*, New York: McGraw-Hill Education, 2015.

[5] D. Neamen, *Microelectronics, Circuit Analysis and Design, 3rd ed.*, New York: McGraw-Hill, 2007.

[6] P. Horowitz and W. Hill, *The Art of Electronics, 3rd ed.*, New York: Cambridge University Press, 2015.

[7] V. Gaudet and K. C. Smith, *Laboratory Explorations to Accompany Microelectronic Circuits, 7th ed.*, New York: Oxford University Press, 2015.

[8] R. Boylestad and L. Nashelesky, *Laboratory Manual for Electronic Devices and Circuit Theory, 7th ed.*, Upper Saddle River, NJ: Prentice-Hall Inc., 1999.

[9] P. Schers and S. Monk, *Practical Electronics for Inventors, 3rd ed.*, New York: McGraw-Hill Education, 2013.

[10] S. Monk, Hacking electronics, New York: McGraw-Hill, 2013.

[11] F. Mims III, *Electronic sensor circuits & Projects*, Niles, IL: Master Publishing Inc., 2007.

[12] F. Mims III, *Engineer's Notebook*, Eagle Rock, Virginia: LLH Master Publishing, 1992.

Appendix C

November 2014

1N4001 - 1N4007
General-Purpose Rectifiers

Features

- Low Forward Voltage Drop
- High Surge Current Capability

DO-41
COLOR BAND DENOTES CATHODE

Ordering Information

Part Number	Top Mark	Package	Packing Method
1N4001	1N4001	DO-204AL (DO-41)	Tape and Reel
1N4002	1N4002	DO-204AL (DO-41)	Tape and Reel
1N4003	1N4003	DO-204AL (DO-41)	Tape and Reel
1N4004	1N4004	DO-204AL (DO-41)	Tape and Reel
1N4005	1N4005	DO-204AL (DO-41)	Tape and Reel
1N4006	1N4006	DO-204AL (DO-41)	Tape and Reel
1N4007	1N4007	DO-204AL (DO-41)	Tape and Reel

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Values are at T_A = 25°C unless otherwise noted.

Symbol	Parameter	Value							Unit
		1N 4001	1N 4002	1N 4003	1N 4004	1N 4005	1N 4006	1N 4007	
V_{RRM}	Peak Repetitive Reverse Voltage	50	100	200	400	600	800	1000	V
$I_{F(AV)}$	Average Rectified Forward Current .375 " Lead Length at T_A = 75°C	1.0							A
I_{FSM}	Non-Repetitive Peak Forward Surge Current 8.3 ms Single Half-Sine-Wave	30							A
I^2t	Rating for Fusing (t < 8.3 ms)	3.7							A^2sec
T_{STG}	Storage Temperature Range	-55 to +175							°C
T_J	Operating Junction Temperature	-55 to +175							°C

Thermal Characteristics

Values are at $T_A = 25°C$ unless otherwise noted.

Symbol	Parameter	Value	Unit
P_D	Power Dissipation	3.0	W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	50	°C/W

Electrical Characteristics

Values are at $T_A = 25°C$ unless otherwise noted.

Symbol	Parameter	Conditions	Value	Unit
V_F	Forward Voltage	$I_F = 1.0$ A	1.1	V
I_{rr}	Maximum Full Load Reverse Current, Full Cycle	$T_A = 75°C$	30	µA
I_R	Reverse Current at Rated V_R	$T_A = 25°C$	5.0	µA
		$T_A = 100°C$	50	
C_T	Total Capacitance	$V_R = 4.0$ V, f = 1.0 MHz	15	pF

Typical Performance Characteristics

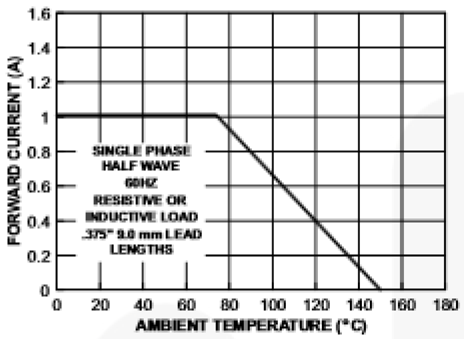


Figure 1. Forward Current Derating Curve

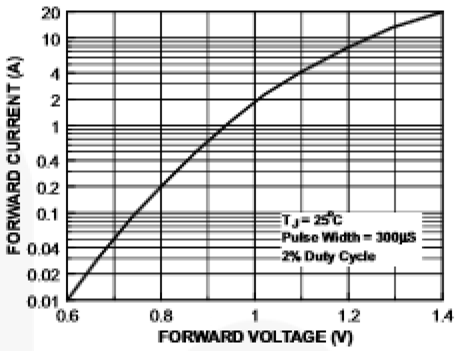


Figure 2. Forward Characteristics

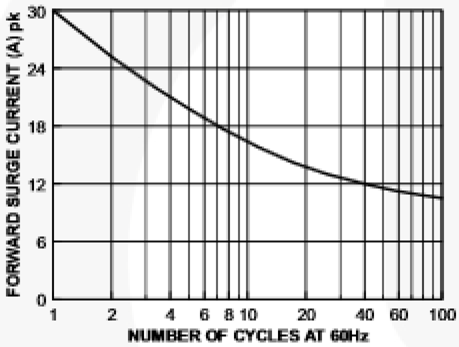


Figure 3. Non-Repetitive Surge Current

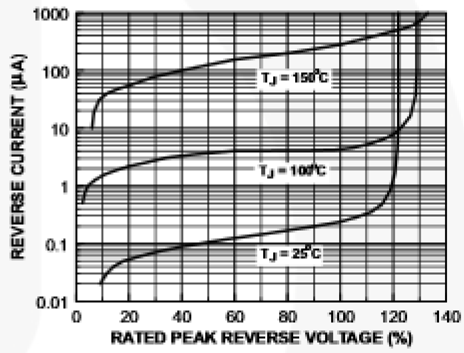


Figure 4. Reverse Characteristics

Appendix D

ZENER DIODE TABLE								
Volt	0.4 Watt		0.5 Watt		1 Watt		5 Watt	
2.4			1N5221	1N4617		UZ87=UZ88		UZ51=52=53
2.5			1N5222			UZ81=UZ82		UZ57=58=59
2.7			1N5223	1N4618				
2.8			1N5224					
3.0			1N5225	1N4619				
3.3	1N746		1N5226	1N4620	1N4728		1N5333	
3.6	1N747		1N5227	1N4621	1N4729		1N5334	
3.9	1N748		1N5228	1N4622	1N4730		1N5335	
4.3	1N749		1N5229	1N4623	1N4731		1N5336	
4.7	1N750		1N5230	1N4624	1N4732		1N5337	
5.1	1N751		1N5231	1N4625	1N4733		1N5338	
5.6	1N752		1N5232	1N4626	1N4734		1N5339	
6.0			1N5233	1N469			1N5340	
6.2	1N753		1N5234	1N4627	1N4735		1N5341	
6.8	1N754	1N957	1N5235	1N4628	1N4736	UZ8806	1N5342	UZ5806
7.5	1N755	1N958	1N5236	1N4629	1N4737	UZ8807	1N5343	UZ5807
8.2	1N756	1N959	1N5237	1N4630	1N4738	UZ8808	1N5344	UZ5808
8.7			1N5238	1N4695			1N5345	
9.1	1N757	1N960	1N5239	1N4631	1N4739	UZ8809	1N5346	UZ5809
10.0	1N758	1N961	1N5240	1N4632	1N4740	UZ8810	1N5347	UZ5810
11.0		1N962	1N5241	1N4633	1N4741		1N5348	
12.0	1N759	1N963	1N5242	1N4634	1N4742	UZ8812	1N5349	UZ5812
13.0	1N717	1N964	1N5243	1N4635	1N4743	UZ8813	1N5350	UZ5813
14.0			1N5244				1N5351	UZ5814
15.0	1N718	1N965	1N5245	1N4636	1N4744	UZ8815	1N5352	UZ5815
16.0	1N719	1N966	1N5246	1N4637	1N4745	UZ8816	1N5353	UZ5816
17.0			1N5247				1N5354	
18.0	1N720	1N967	1N5248	1N4638	1N4746	UZ8818	1N5355	UZ5818
19.0			1N5249				1N5356	
20.0	1N721	1N968	1N5250	1N4639	1N4747	UZ8820	1N5357	UZ5820
22.0	1N722	1N969	1N5251	1N4640	1N4748	UZ8822	1N5358	UZ5822
24.0	1N723	1N970	1N5252	1N4641	1N4749	UZ8824	1N5359	UZ5824
25.0			1N5253				1N5360	
27.0	1N724	1N971	1N5254	1N4642	1N4750	UZ8827	1N5361	UZ5827
28.0			1N5255				1N5362	
30.0	1N725	1N972	1N5256	1N4643	1N4751	UZ8830	1N5363	UZ5830
33.0	1N726	1N973	1N5257	1N4644	1N4752	UZ8833	1N5364	UZ5833
36.0	1N727	1N974	1N5258	1N4645	1N4753	UZ8836	1N5365	UZ5836
39.0	1N728	1N975	1N5259	1N4646	1N4754	UZ8840	1N5366	UZ5840
43.0	1N729	1N976	1N5260	1N4647	1N4755		1N5367	
47.0	1N730	1N977	1N5261	1N4648	1N4756	UZ8845	1N5368	
51.0	1N731	1N978	1N5262		1N4757	UZ8850	1N5369	UZ5850
56.0	1N732	1N979	1N5263		1N4758	UZ8856	1N5370	UZ5856
60.0			1N5264				1N5371	UZ5860
62.0	1N733	1N980	1N5265		1N4759	UZ8860	1N5372	
68.0	1N734	1N981	1N5266		1N4760	UZ8870	1N5373	
75.0	1N735	1N982	1N5267		1N4761	UZ8875	1N5374	UZ5875
82.0	1N736	1N983	1N5268		1N4762	UZ8880	1N5375	UZ5880
87.0			1N5269				1N5376	
91.0	1N737	1N984	1N5270		1N4763	UZ8890	1N5377	UZ5890
100.0	1N738	1N985	1N5271		1N4764	UZ8110	1N5378	UZ5310
110.0	1N739	1N986	1N5272			UZ8111	1N5379	UZ5311
120.0	1N740	1N987	1N5273			UZ8112	1N5380	UZ5312
130.0	1N741	1N988	1N5274			UZ8113	1N5381	UZ5313
140.0			1N5275			UZ8114	1N5382	UZ5314
150.0	1N742	1N989	1N5276			UZ8115	1N5383	UZ5315
160.0	1N743	1N990	1N5277			UZ8116	1N5384	UZ5316
170.0			1N5278			UZ8117	1N5385	UZ5317
180.0	1N744	1N991	1N5279			UZ8118	1N5386	UZ5318
190.0			1N5280			UZ8119	1N5387	UZ5319
200.0	1N745	1N992	1N5281			UZ8120	1N5388	UZ5320

Appendix E

Standard Components Values

Standard Resistor Values (±5%)						
1.0	10	100	1.0K	10K	100K	1.0M
1.1	11	110	1.1K	11K	110K	1.1M
1.2	12	120	1.2K	12K	120K	1.2M
1.3	13	130	1.3K	13K	130K	1.3M
1.5	15	150	1.5K	15K	150K	1.5M
1.6	16	160	1.6K	16K	160K	1.6M
1.8	18	180	1.8K	18K	180K	1.8M
2.0	20	200	2.0K	20K	200K	2.0M
2.2	22	220	2.2K	22K	220K	2.2M
2.4	24	240	2.4K	24K	240K	2.4M
2.7	27	270	2.7K	27K	270K	2.7M
3.0	30	300	3.0K	30K	300K	3.0M
3.3	33	330	3.3K	33K	330K	3.3M
3.6	36	360	3.6K	36K	360K	3.6M
3.9	39	390	3.9K	39K	390K	3.9M
4.3	43	430	4.3K	43K	430K	4.3M
4.7	47	470	4.7K	47K	470K	4.7M
5.1	51	510	5.1K	51K	510K	5.1M
5.6	56	560	5.6K	56K	560K	5.6M
6.2	62	620	6.2K	62K	620K	6.2M
6.8	68	680	6.8K	68K	680K	6.8M
7.5	75	750	7.5K	75K	750K	7.5M
8.2	82	820	8.2K	82K	820K	8.2M
9.1	91	910	9.1K	91K	910K	9.1M

Standard Capacitor Values (±10%)						
10pF	100pF	1000pF	.010µF	.10µF	1.0µF	10µF
12pF	120pF	1200pF	.012µF	.12µF	1.2µF	
15pF	150pF	1500pF	.015µF	.15µF	1.5µF	
18pF	180pF	1800pF	.018µF	.18µF	1.8µF	
22pF	220pF	2200pF	.022µF	.22µF	2.2µF	22µF
27pF	270pF	2700pF	.027µF	.27µF	2.7µF	
33pF	330pF	3300pF	.033µF	.33µF	3.3µF	33µF
39pF	390pF	3900pF	.039µF	.39µF	3.9µF	
47pF	470pF	4700pF	.047µF	.47µF	4.7µF	47uF
56pF	560pF	5600pF	.056µF	.56µF	5.6µF	
68pF	680pF	6800pF	.068µF	.68µF	6.8µF	
82pF	820pF	8200pF	.082µF	.82µF	8.2µF	

Appendix F

Guidelines for Writing EE 312 Reports

Your reports should be computer-typed and spell-checked. Paragraphs should be written in Times New Roman, size 14 points and headings should be bolded, size 14 points. Use formal English, direct language, and simple terms. The following link has good information that might help you to improve your technical writing skills:

https://msu.edu/course/be/485/bewritingguideV2.0.pdf

Use the following checklist to complete the requirements for each experiment:

1- **Cover sheet** which shows the name of the course, the report number, titles of the included experiments, your name, number, section number, and date of submission [2]
2- **Objectives** [2]
3- **Circuit Diagrams** [2]
4- **Measurements**: A descriptive list of all types of measurements that have been taken and the equipment used to take them (e.g., $V_O(t)$ was obtained using an oscilloscope when we applied a 14-$V_{pk\text{-}pk}$ sinusoid to the input–do not copy and paste the procedure!) [2]
5- **Observations** based on your measurements (e.g., I have observed clipping in positive half cycles of $V_O(t)$ when the input was a 14-$V_{pk\text{-}pk}$ sinusoid, but the clipping disappeared when the input's peak to peak amplitude was reduced to 2 V) [4]
6- **Discussion of Observations** where you try to interpret your measurements/data and determine whether or not they are consistent with theory (e.g., the clipping in $V_O(t)$ is due to D_1 operating in the forward region and hence acting approximately as a battery of value 0.7 V) [4]
7- A **conclusion** that includes a paragraph about meeting the objectives of the experiment [4]
8- Any comments you would like to add (e.g., it would be interesting to carry out the same experiment with a Ge diode in place of the Si diode–in that case I would expect $V_O(t)$ to look like this:…) [Bonus]
9- **References** (if applicable)
10- Attachment of all of your lab worksheets that contain the details of your measurements and post measurement calculations in the **appendix** [20]