

King Saud University College of Engineering Electrical Engineering Department 2nd Semester 1427H/1428H EE208: Logic Design Final Term Exam Time Allowed: 3H) 208

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Attempt All Questions

Question One

- a) Convert $(010111.01011)_{BCD}$ to Binary, Octal and HEX.
- b) Implement the following logic function using only NAND gates:

F (**A**, **B**, **C**) = $[A \oplus (\overline{B \oplus C})]$

Question Two

A logic circuit receives 5 bits BCD code and outputs the equivalent binary code.

- a) Develop the truth table to implement the circuit.
- b) Draw the circuit diagram using decoders and logic gates
- c) Compute the ROM size required to implement the above circuit

Question Three

A Logic circuit has two input codes A, B and an output code F. Each code consists of 4 bits. The circuit has two control inputs x and y to implement the following operations:

Control Inputs	
ХҮ	Operation
0 0	A+B addition
0 1	A-B subtraction
1 0	A+1 increment
1 1	A-1 decrement

Design the circuit using 4 bits parallel adder chip

Question Four

A sequential circuit consists of a one JK- Flip flop and Full subtractor (FS) with two inputs X and Y. The circuit has one output B_0 as shown in the block diagram below.

- a) Construct the truth table for the full subtractor.
- b) Derive the state table and state diagram.
- c) Derive the minimized state equation for Q^+ .



Question Five:

A digital system has a clock generator that produces pulses at a frequency of 1 KHz. Design a counter circuit that provides a clock with a cycle time of 0.05 second.

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