



CSC 220: Computer Organization

Unit 0 Introduction



Course Introduction

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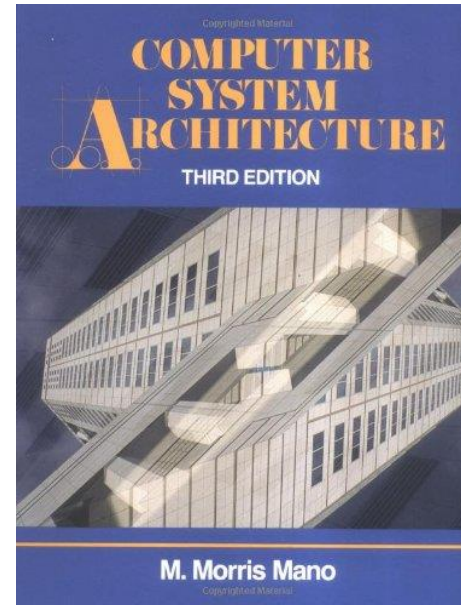
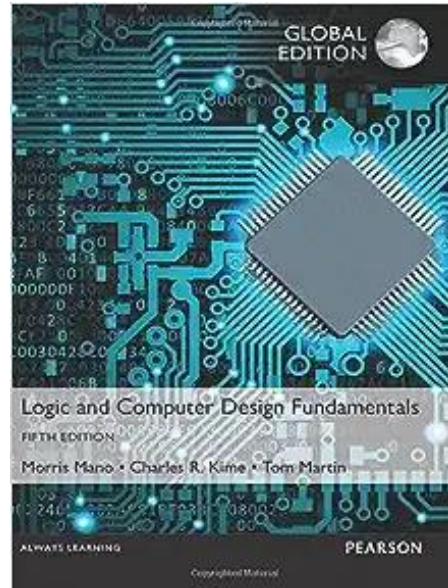
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Course Introduction

Text Books

1. M. Morris Mano, Charles R. Kime and Tom Martin, **Logic and Computer Design Fundamentals**, 5th (Global) Edition, Pearson Education Limited, 2016. ISBN: 9781292096124
2. Morris Mano, **Computer System Architecture** - 3rd Edition, Publisher: McGraw Hill



Class Note based on the main text (Available at the LMS)

Course Introduction

CSC220 - Computer Organization (2-2-1) - Required Course

Pre-requisites: **MATH 151** - Discrete Mathematics

Topics

- Data Representation: binary number systems, signed number systems, use of 1's and 2's complements in addition and subtraction
- Logic gates, Logic function, K-Map simplification
- Combinational circuits: Multiplexer, De-multiplexer, Decoder, Arithmetic circuits
- Sequential circuits: register, binary counters, and memory organization
- Arithmetic and Logic Unit design, Central Processing Unit design
- Register, Register Transfer Language, and micro-operations instruction set
- CPU design and programming

Course Introduction

CSC 220: Course Learning Outcomes

Upon completing CSC220, students should be able to:

1. Write a simplified logic function
2. Design combinational circuits such as Adder, Multiplexer, Decoder
3. Identify different components of a computer system (e.g. ALU, registers, RAM, Control Unit)
4. Design a basic Arithmetic and Logic Unit (ALU)
5. Recognize appropriate combinational and sequential circuits for CPU design
6. Describe instruction set architecture
7. Write simple program in register transfer language (RTL) and assembly language

Course Introduction

Assessment Methods:

Assessment	Grades
Homework	5%
Midterm1	25%
Quiz	10%
Project + Lab Evaluation	10%
Final Lab	10%
Final Exam	40%

Important Dates

Exam	Date	time
Midterm Exam	Wednesday, February 19, 2025	12:00-1:30
Quiz	Sunday, April 20, 2025	12:00-12:50
Lab Exam	Monday, April 28, 2025	12:00-1:30
Final Exam	Tuesday, May 27, 2025	8:00-11:00

Course Introduction

Course Plan (tentative)

		Lecture		Tutorial	LAB	desc
Week	Date	TUES	THU			
1	1/5/2025	Unit-1Number System	Unit-1Number System	Orientation+Introduction		
2	1/12/2025	Unit-2 Digital Circuit Design	Unit-2 Digital Circuit Design	T1-Number System	Introduction	
3	1/19/2025	Unit-3 Simplification	Unit-3 Simplification	T2-Logic Circuit Design	Lab1 Logic gates	
4	1/26/2025	Unit-4 Signed Number Representation	Unit-4 Signed Number Representation	T3-Kmap	Lab2_Kmap	
5	2/2/2025	Unit-5 Combinational Circuit-1	Unit-5 Combinational Circuit-1	T4- Number Representation		
6	2/9/2025	Unit-6 Combinational Circuit-2	Unit-6 Combinational Circuit-2	T5-Combinational Ckt 1-Adder	Lab3_Adder	
7	2/16/2025	Unit-7 Sequencial Circuit	Unit-7 Sequencial Circuit	T6-Combinational Ckt 2 MUX,Decoder	Lab4 MUX Decoder	
8	2/23/2025	Unit-8 Registers & RTL	Unit-8 Registers & RTL	No Tutorial due to FHD		
9	3/2/2025	Unit-9 Counters & RAM	Unit-9 Counters & RAM	T7-Flip Flop /T8- Registers & RTL	Lab6 Register	
10	3/9/2025	Unit-9 Counters & RAM	Unit-9 Counters & RAM	T8- Registers & RTL		
11	3/16/2025	Eid Alfiter BREAK				
12	3/23/2025					
13	3/30/2025					
14	4/6/2025	Unit-10 ALU Design	Unit-10 ALU Design	T8- Registers & RTL /T9-Counter-RAM	Lab7_Counter	
15	4/13/2025	Unit-11 Datapath Design	Unit-11 Datapath Design	T10-ALU	Lab8 AU	
16	4/20/2025	Unit-12 CPU Design & Programming	Unit-12 CPU Design & Programming	T11 -Datapath Design	Lab9_ALU+Shifter	
17	4/27/2025			T12 -CPU Programming		
18	5/4/2025					
19	5/11/2025					
20	5/18/2025					
21	5/25/2025	Final EXAM 27-5-2025				

Course Introduction

Assessment	Grades	due-date	
		date	time
HW1	2%	Thursday, 13 February 2025	11:59 PM
HW2	3%	Thursday, April 17, 2025	11:59 PM
Midterm1	25%	Wednesday, February 19, 2025	12:00-1:30
Quiz	10%	Sunday, April 20, 2025	12:00-1:00
Project	5%	Thursday, April 24, 2025	11:59 PM
Lab EXAM	10%	Monday, April 28, 2025	10:00-11:30
Final Exam	40%	Tuesday, May 27, 2025	8:00-11:00
Weekly Evaluation	5%	Every Week starting from second week	

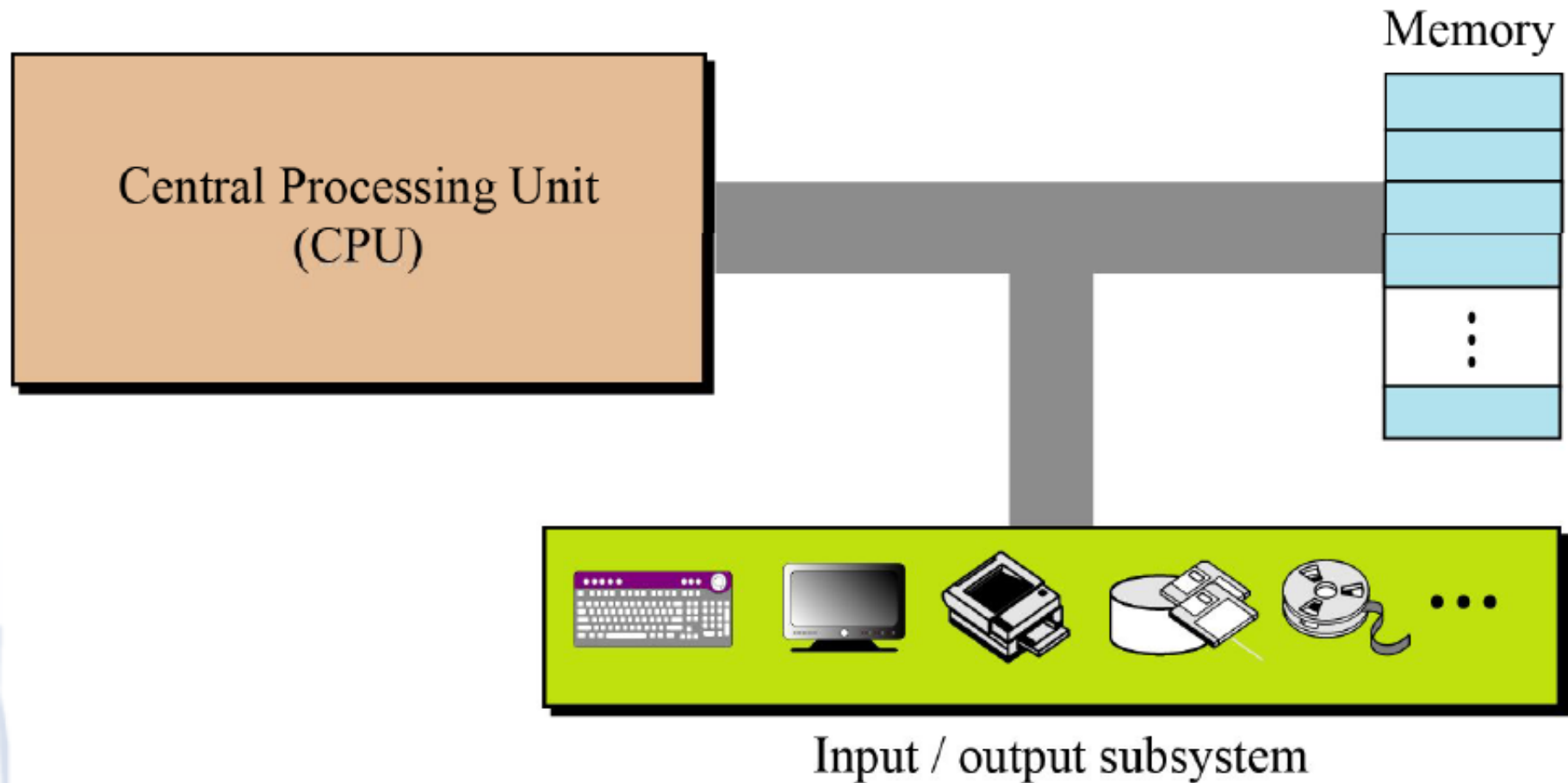
Course Introduction

Attendance Rules

- **Student must attend 75% of lectures.**
- **Student is the responsible about counting her absence.**
- **Student must enter the lecture room BEFORE the lecture starts.**
- **If student decides to miss a lecture for personal reasons, no action needed.**
- **If a student missed the midterm or final exams, she should contact the exam committee;**
- **if a student missed a quiz, or lab evaluation no backup.**

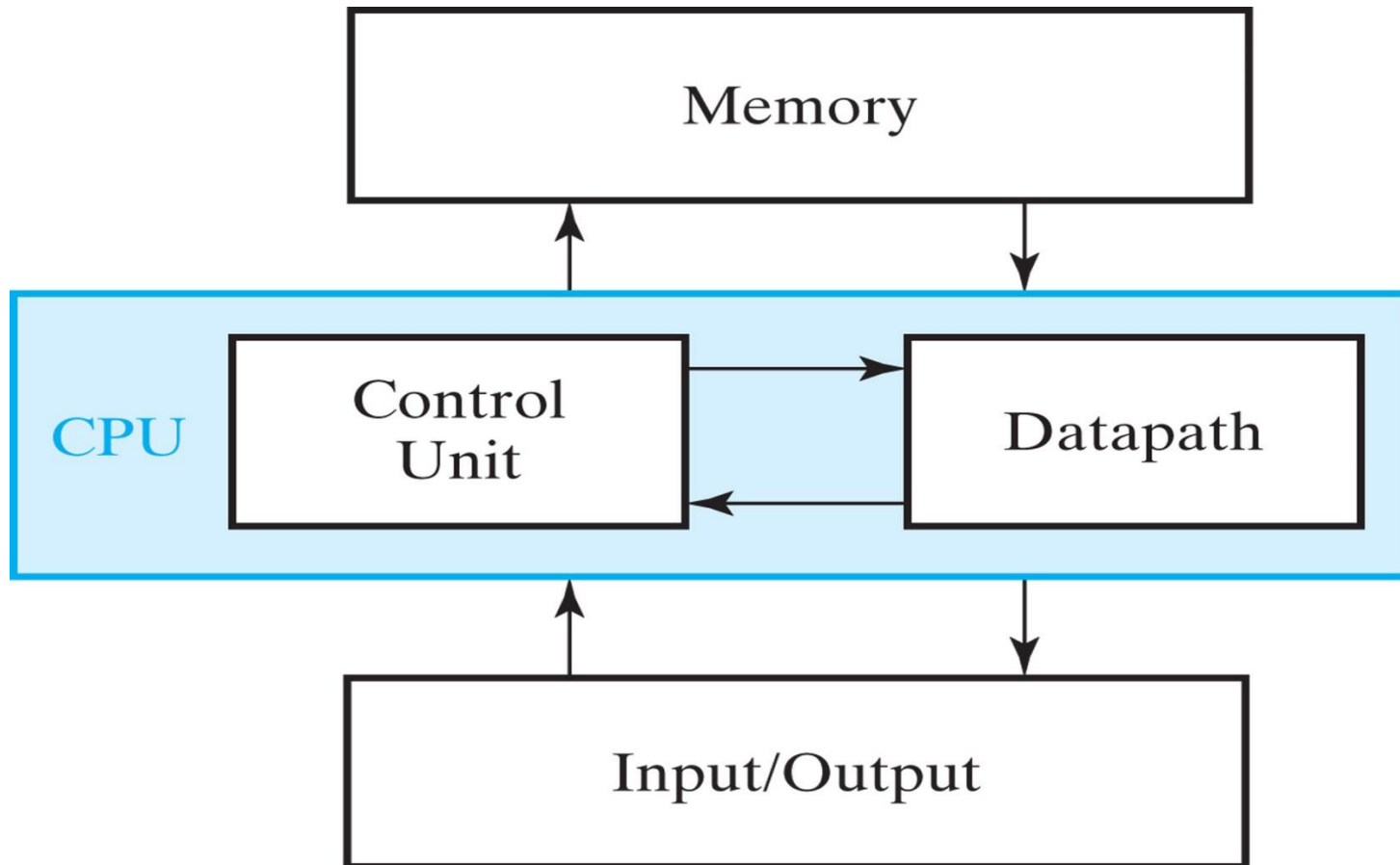
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Computer Hardware (Subsystems)



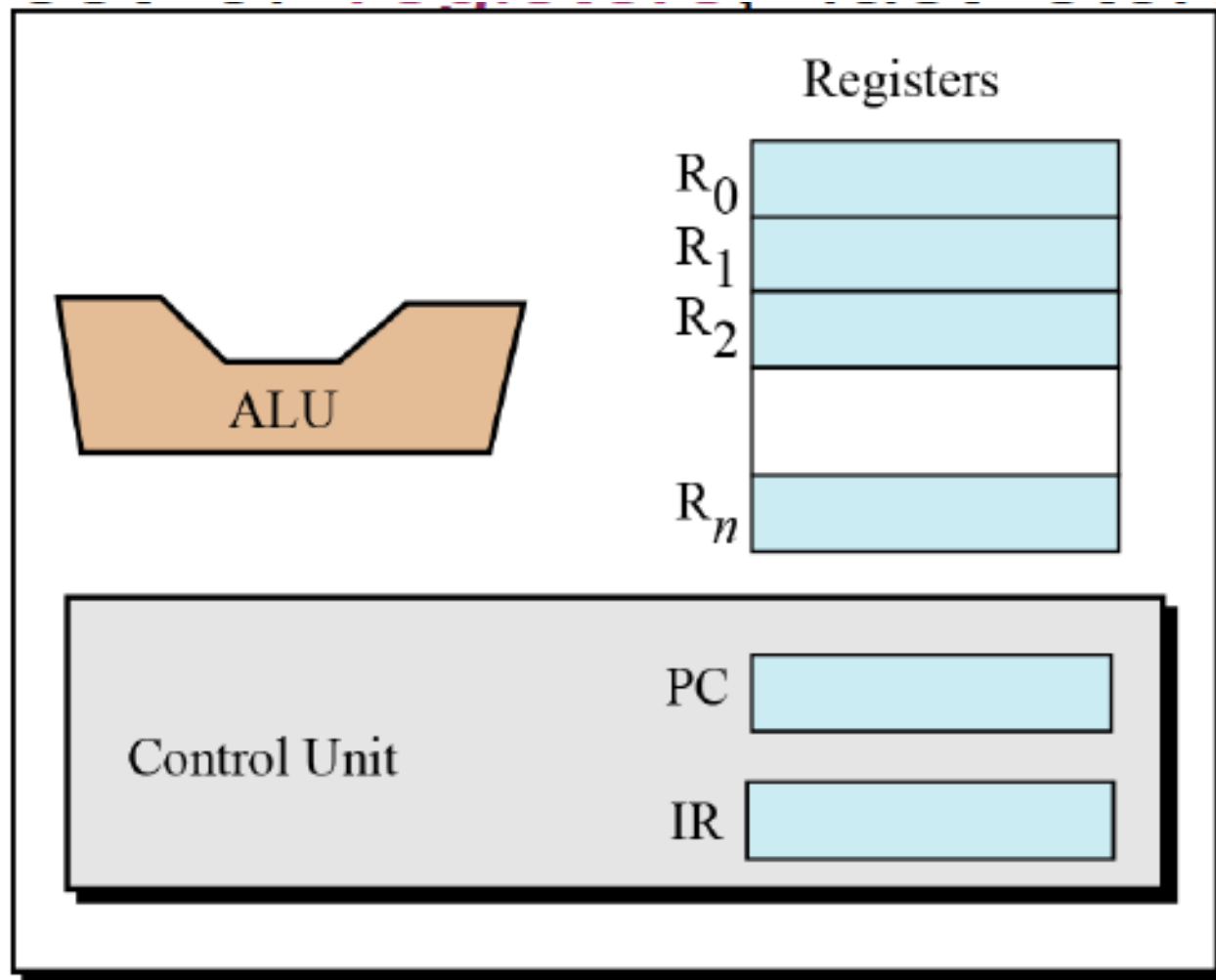
Course Introduction

A Digital Computer



Course Introduction

Central Processing Unit (CPU)



Course Introduction

Layers of Abstraction

Algorithms
Programming Languages
Operating Systems
Instruction Set Architecture
Microarchitecture
Register Transfers
Logic Gates
Transistor Circuits

□ **FIGURE 1-5**

Typical Layers of Abstraction in Modern Computer Systems

First Generation (1951–57)

First Generation- Vacuum Tubes

ENIAC: Generally regarded as the first electronic computer:

Programmed by manually setting switches

full **Electronic Numerical Integrator and Computer**

vacuum tube :made
of glass, size of
lightbulbs

weighed 30 tons

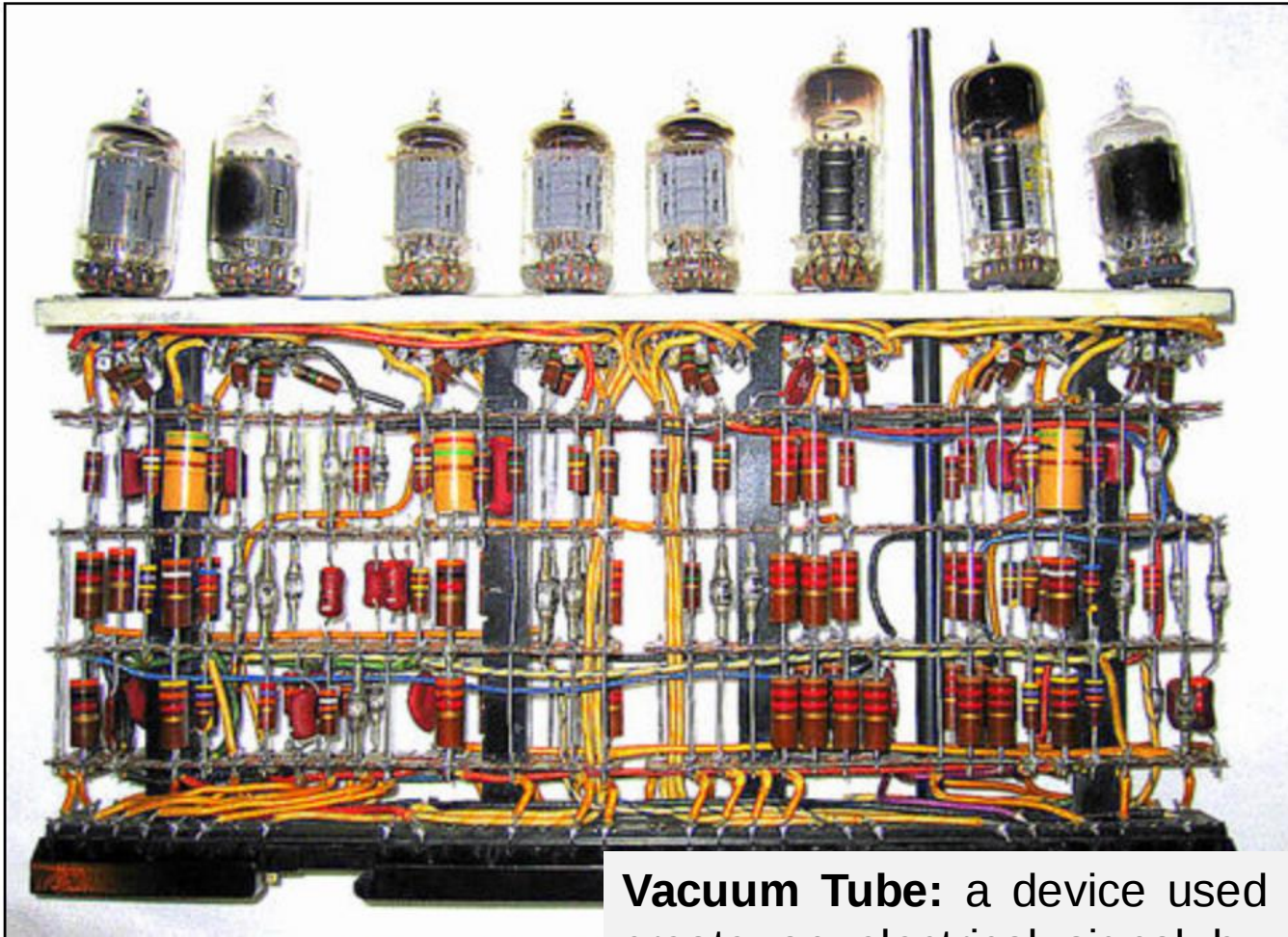


proposal was accepted
in 1943, not finished
until 1946

Purpose: break a
coded message,
calculate range tables
for aiming its heavy
artillery

First Generation (1951–57)

Vacuum Tubes from an early 1950's IBM Computer



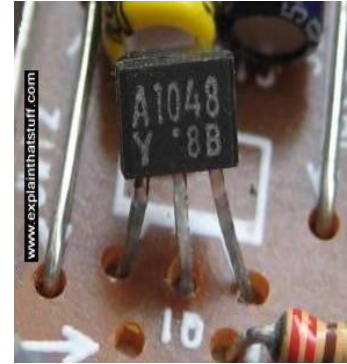
An IBM computer vacuum

Vacuum Tube: a device used to amplify, switch, modify, or create an electrical signal by controlling the movement of electrons in a low-pressure (vacuum) space

Second Generation (1958–63)

Second Generation-Transistors

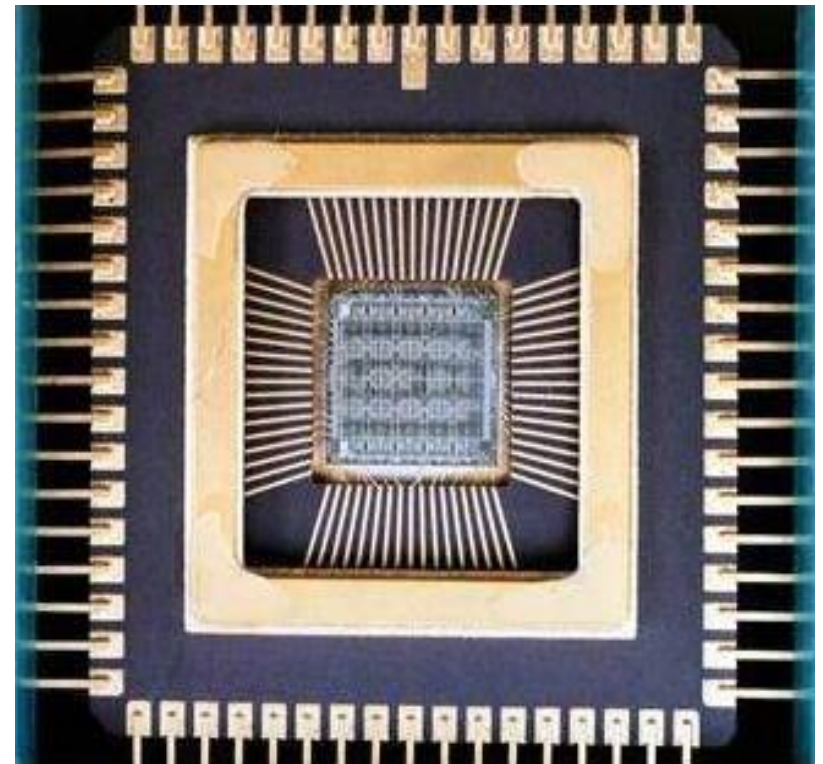
- Transistor was Invented 1947 at Bell Labs
 - small devices that transfer electronic signals across a resistor.
- Replaced vacuum tube
- **Advantages:**
 - Smaller
 - Cheaper
 - Less heat dissipation
 - More reliable
 - Six times faster



Third Generation (1964–690

Third Generation-Integrated Circuits

- Integrated Circuits (IC's): a complete electronic circuit on a small chip made of silicon, in place of transistor
- **Advantages:**
 - More reliable
 - Smaller size
 - Generate less heat
 - Faster
 - Lesser maintenance
 - Still costly
 - Consumed lesser electricity
 - Support high level language



Fourth Generation (1970–90)

Fourth Generation- Very Large Scale Integration VLSI

- Chips containing thousands of transistors on a square centimeter of silicon
- the age of the personal computer
- **Advantages:**
 - Very cheap
 - Portable and reliable
 - Very small size
 - Pipeline processing

Fifth Generation (1991–2021 and beyond)

Fifth Generation: Ultra Large Scale Integration

- ▶ Millions of transistors on a single silicon semiconductor microchip.
- ▶ Advancement in Parallel Processing
- ▶ More user friendly interfaces with multimedia features
- ▶ Availability of very powerful and compact computers at cheaper rates
- ▶ Desktop, Laptop, Notebook, Smartphones.

Course Introduction

Main Component

<https://www.youtube.com/watch?v=yRmPTbGBqVI>

Integrated Circuit (IC) Fabrication

<https://www.youtube.com/watch?v=aWVywhzuHnQ>

<https://www.youtube.com/watch?v=qm67wbB5Gml>

Course Introduction

History of Intel x86 processors

- **4004**: 4-bit processor; 8-bit processors 8080, 8085.
- **8086**: 16-bit processors, introduced in 1979: 20-bit address bus (AB), 16-bit data bus (DB), 5/8/10 MHz.
- **80186**: a faster version of the 8086. Also 20-bit AB and 16-bit DB. Never widely used in computer systems.
- **80286**: introduced in 1982, It has a 24-bit AB, which implies 16MB of memory address space.
- **80386**: Intel introduced its first 32-bit processor in the 1985. It has 32-bit AB and 32-bit DB. It follows their 32-bit architecture known as IA-32.
- **Pentium**: was introduced in 1993 (20th anniversary). it uses a 64-bit wide DB, 60/66 MHz.
- **Itanium**: 64-bit processor, released in 2001; formerly called IA-64, the Itanium uses a 64-bit AB to provide substantially larger address space. Its DB is 128 bits wide.

