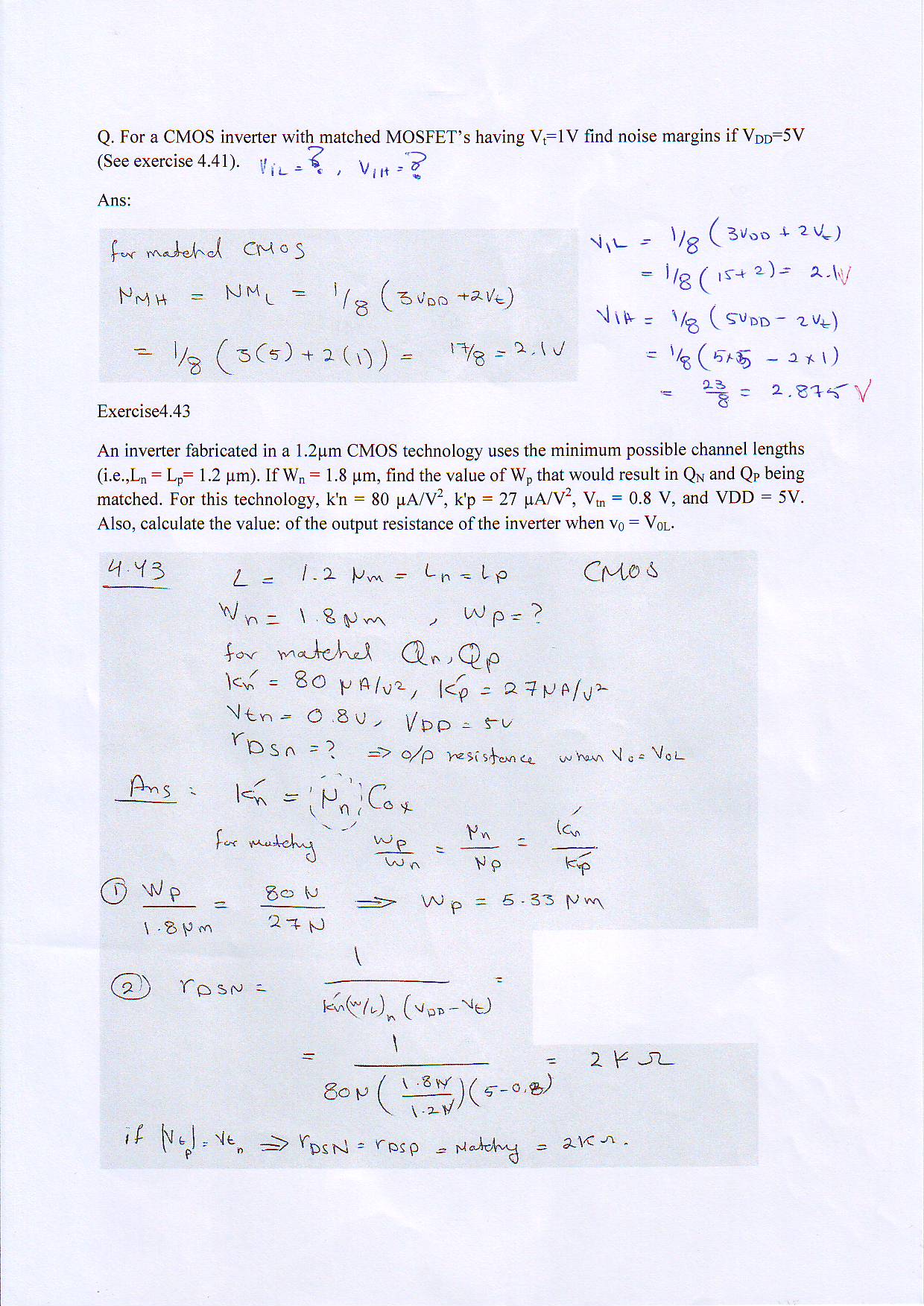


Q. For a CMOS inverter with matched MOSFET’s having Vt=1V find noise margins if VDD=5V. Find VIL, VIH. (See exercise 4.41).

Exercise4.43

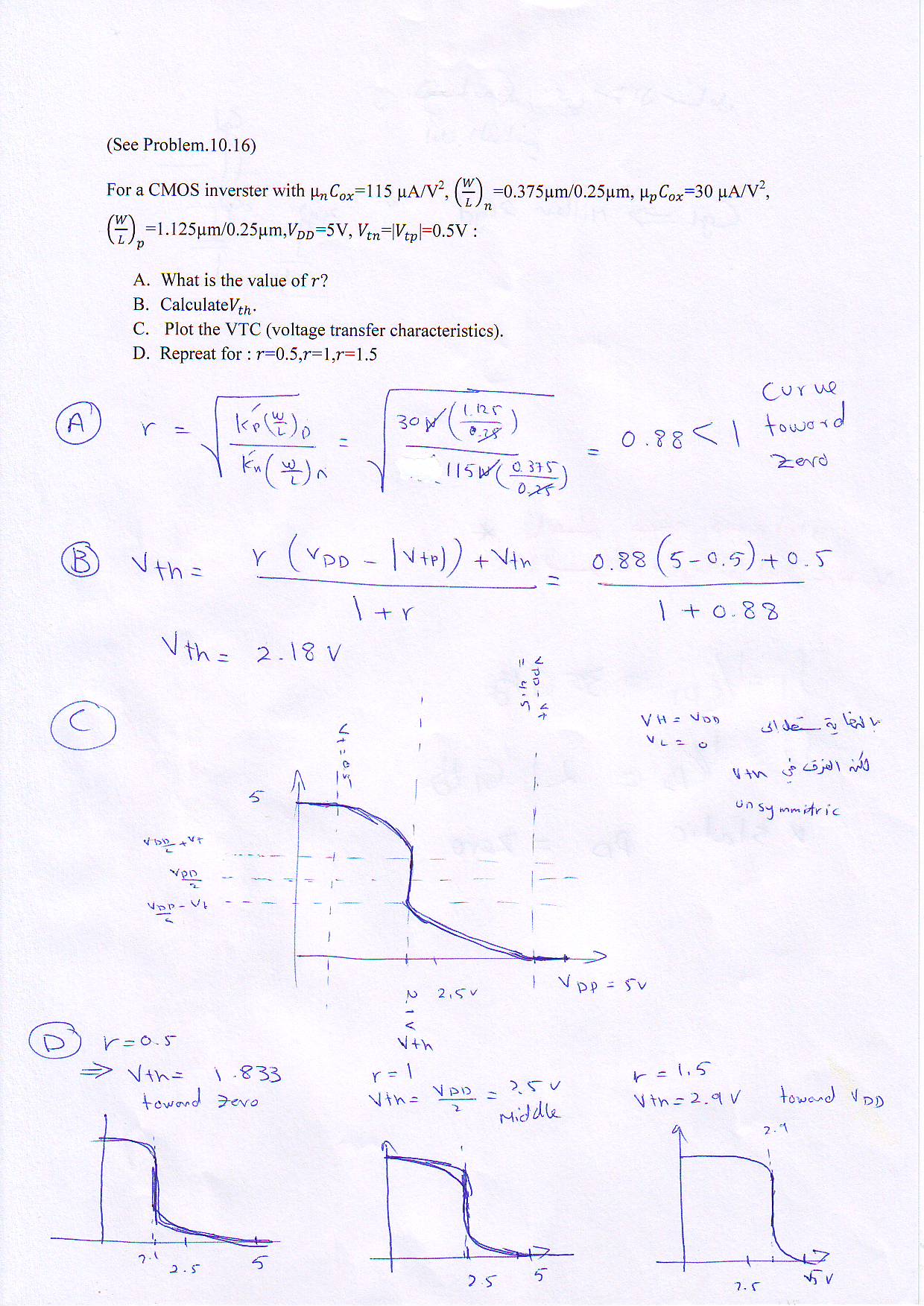
An inverter fabricated in a 1.2µm CMOS technology uses the minimum possible channel lengths (i.e.,Ln = Lp= 1.2 µm). If Wn = 1.8 µm, find the value of Wp that would result in QN and QP being matched. For this technology, k'n = 80 µA/V2, k'p = 27 µA/V2, Vtn = 0.8 V, and VDD = 5V. Also, calculate the value: of the output resistance of the inverter when v0 = V0L.

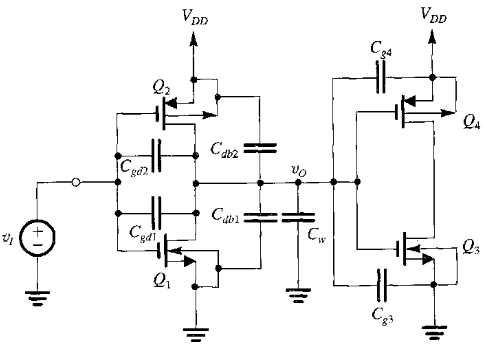


(See Problem.10.16)

For a CMOS inverster with =115 µA/V2, =0.375µm/0.25µm, =30 µA/V2, =1.125µm/0.25µm,=5V, =||=0.5V :

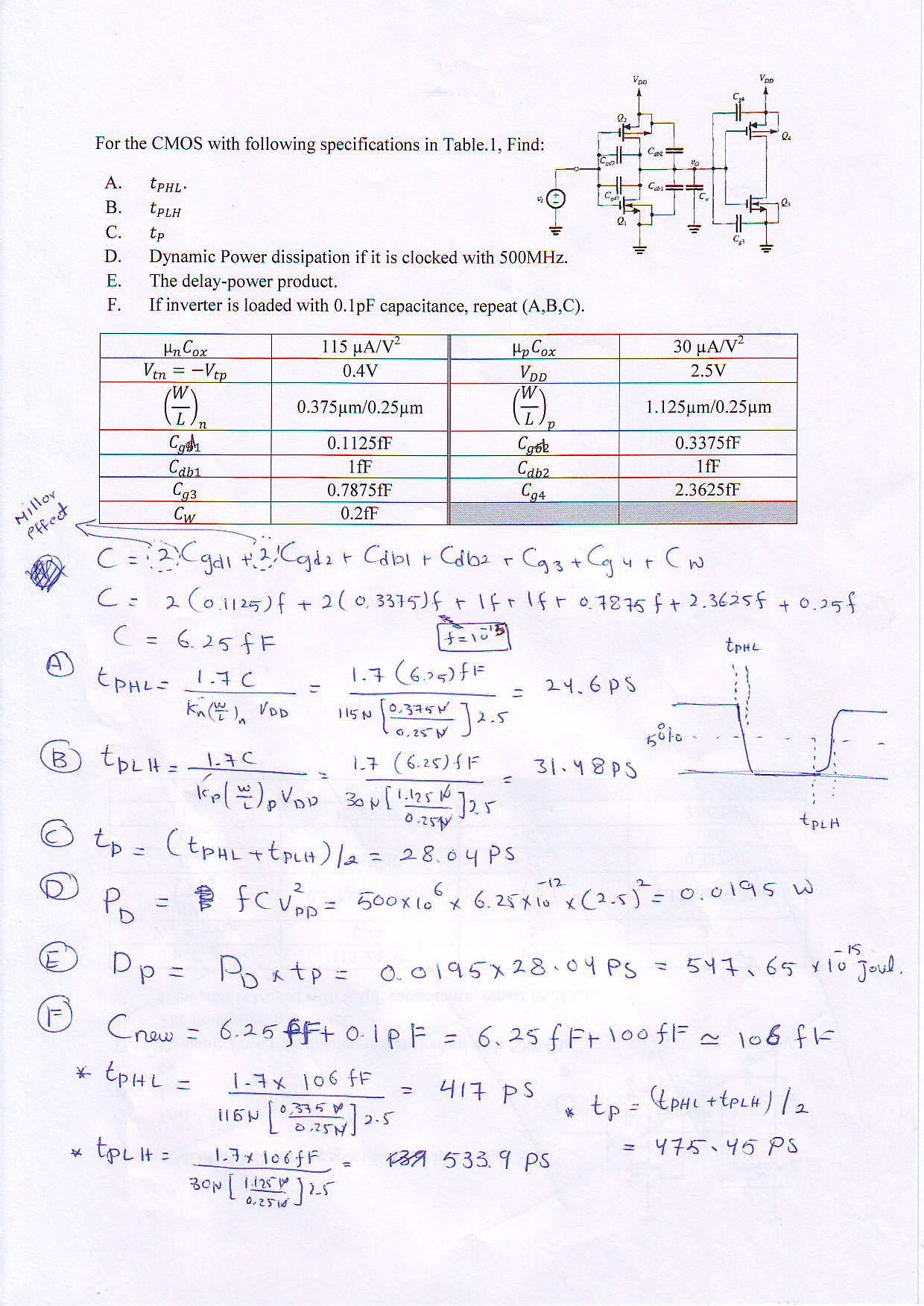
1. What is the value of ?
2. Calculate.
3. Plot the VTC (voltage transfer characteristics).
4. Repreat for : =0.5,=1,=1.5



For the CMOS with following specifications in Table.1, Find:

1. .
2. Dynamic Power dissipation if it is clocked with 500MHz.
3. The delay-power product.
4. If inverter is loaded with 0.1pF capacitance, repeat (A,B,C).

|  |  |  |  |
| --- | --- | --- | --- |
|  | 115 µA/V2 |  | 30 µA/V2 |
|  | 0.4V |  | 2.5V |
|  | 0.375µm/0.25µm |  | 1.125µm/0.25µm |
|  | 0.1125fF |  | 0.3375fF |
|  | 1fF |  | 1fF |
|  | 0.7875fF |  | 2.3625fF |
|  | 0.2fF |  |  |



EE 401: Quiz

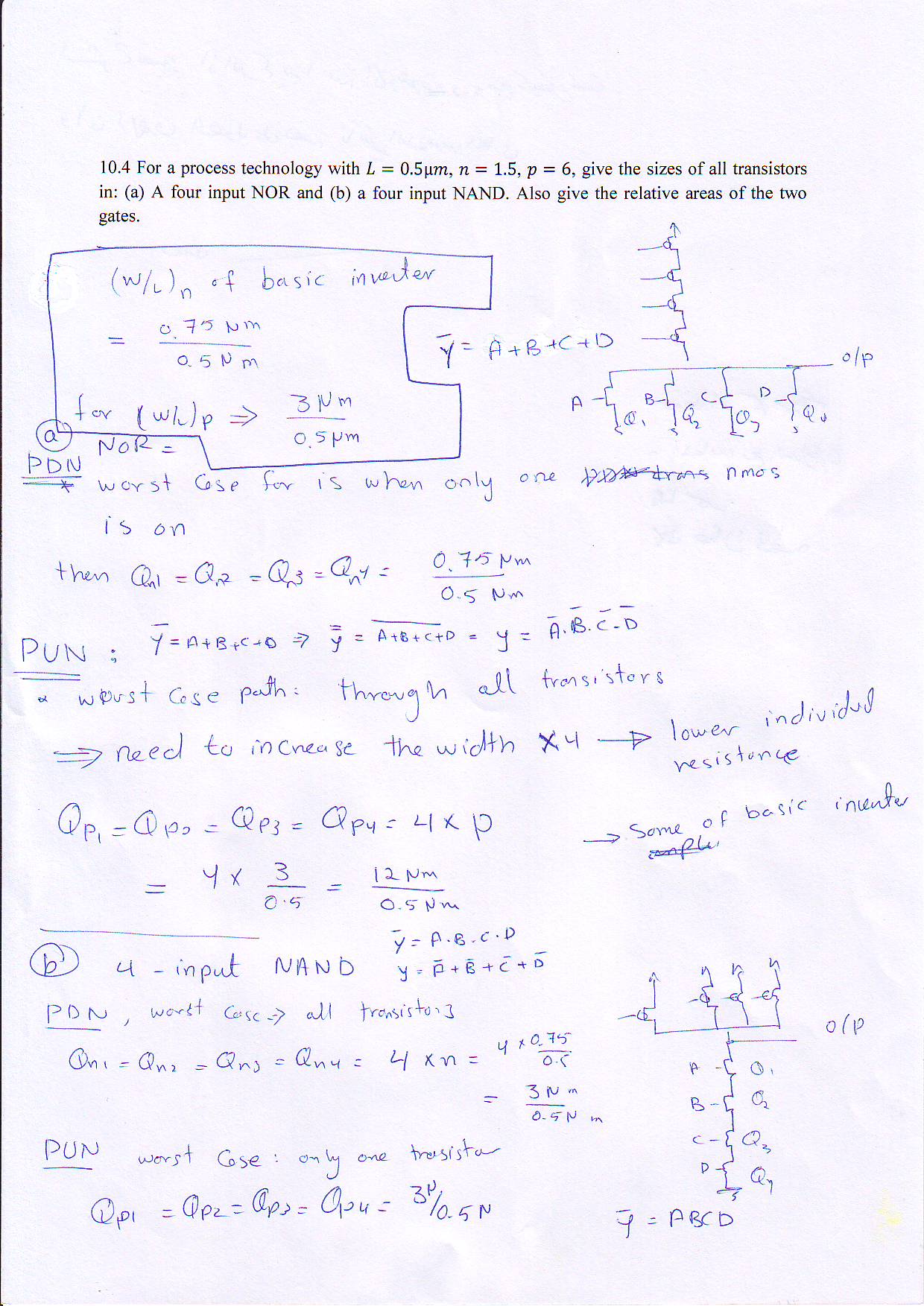
Name (Arabic): Student #

***Question 7:* (6 Pts.)**

|  |
| --- |
| 1. A CMOS inverter has *kn* = *kp* = 330 *µ*A/V2, *VDD* = 3.3V and *Vtn*= – *Vtp* = 0.8 V. 2. Is the inverter matched? Why? 3. For this inverter, what are the values of *VOH*, *VOL* in the VTC curve? 4. Find: *VIH ,VIL*, *Vth*, *NMH*, *NML*, *rDSN and rDSP*. |

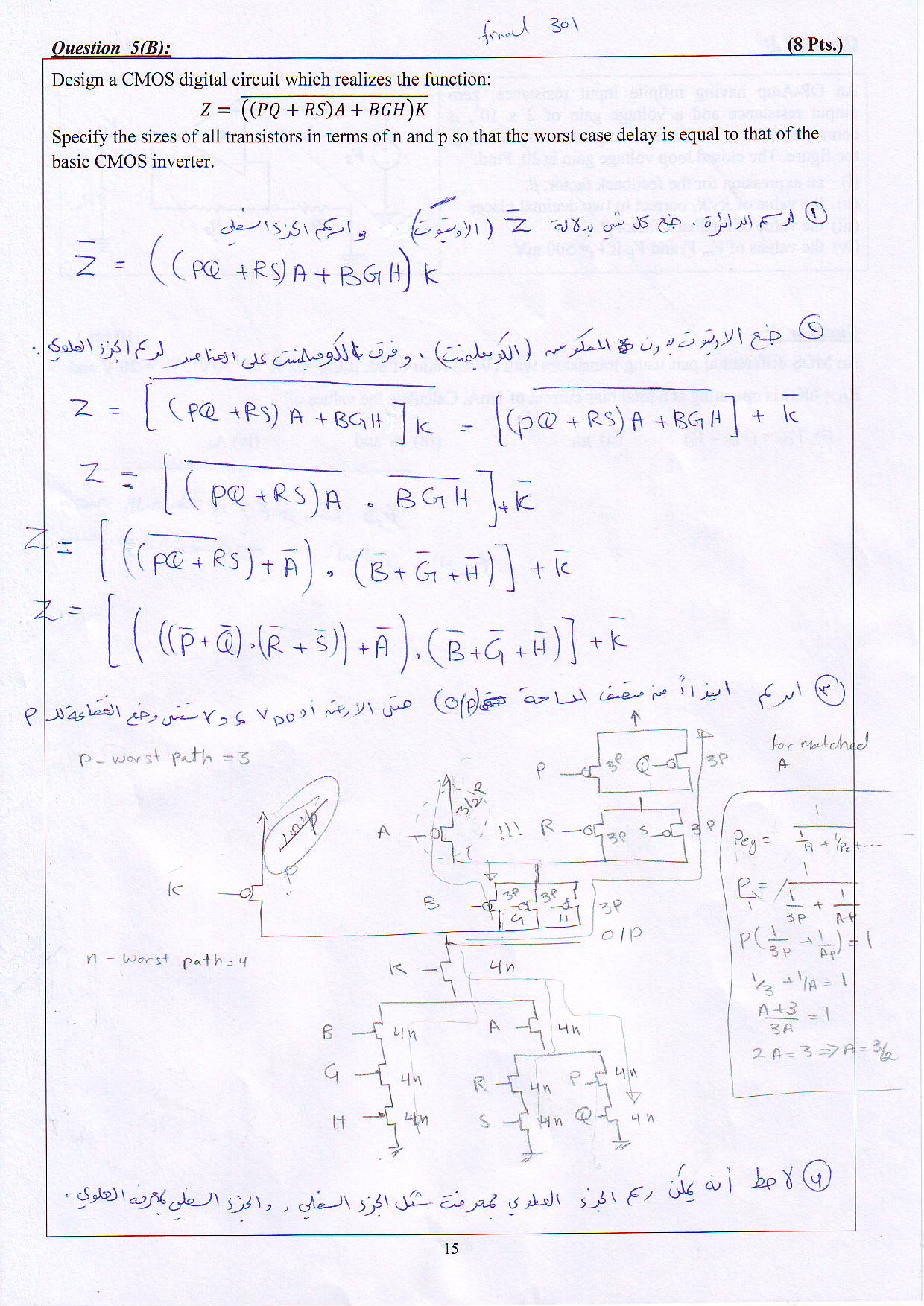


(Exersice10.4) For a process technology with , , , give the sizes of all transistors in: (a) A four input NOR and (b) a four input NAND. Also give the relative areas of the two gates.

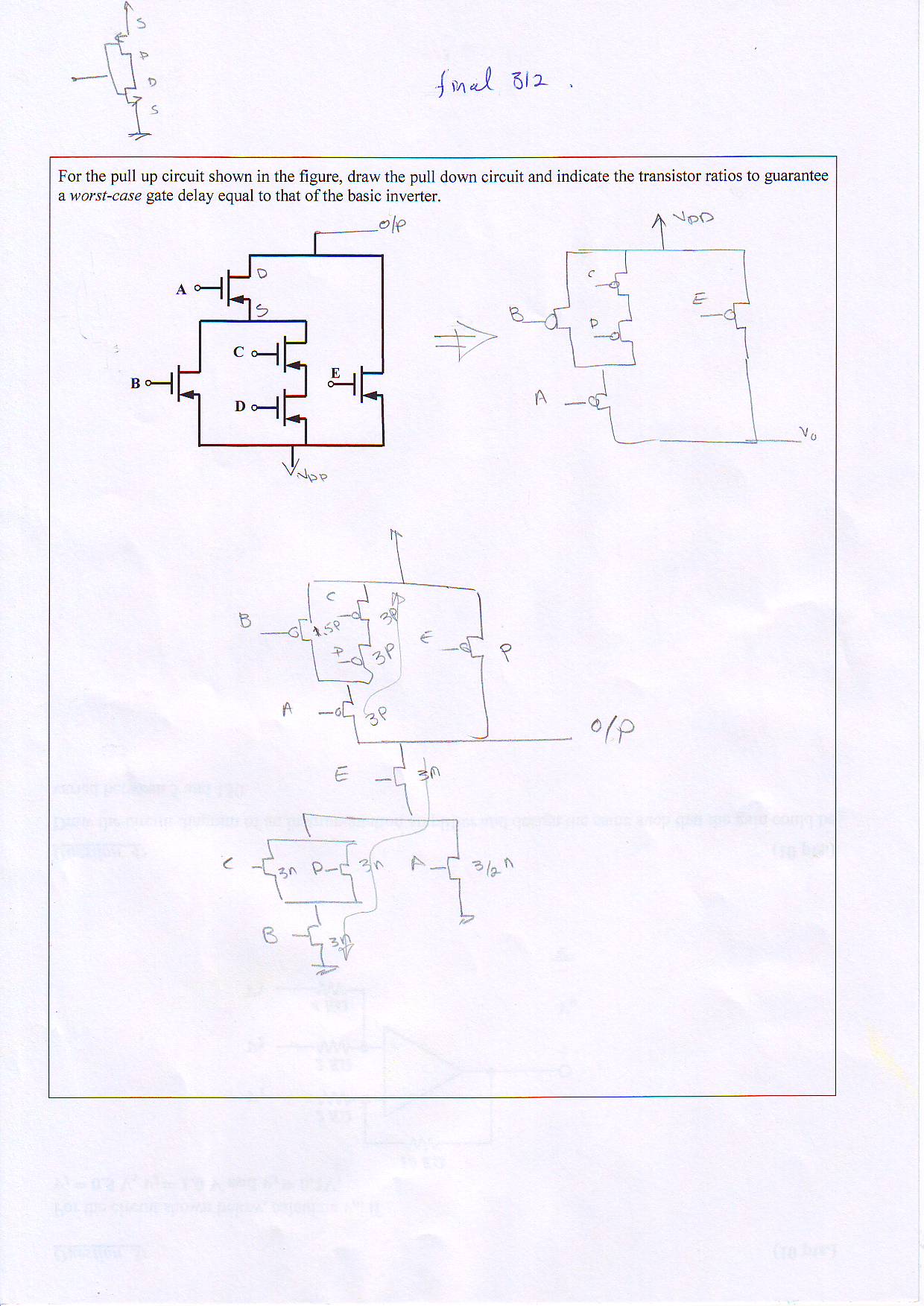


***Question 5(B):* (8 Pts.) (Final 301)**

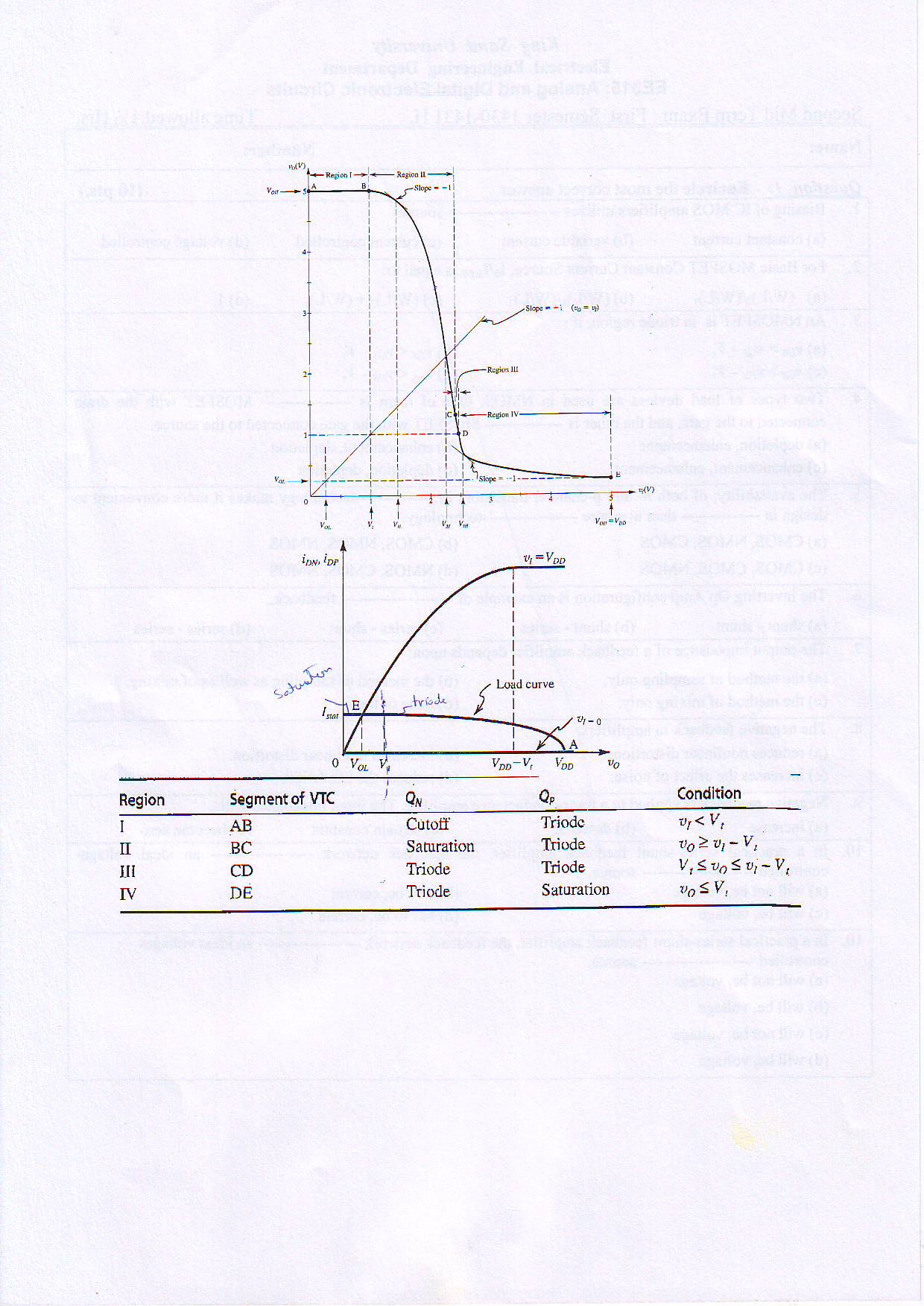
|  |
| --- |
| Design a CMOS digital circuit which realizes the function:  Specify the sizes of all transistors in terms of n and p so that the worst case delay is equal to that of the basic CMOS inverter. |



|  |
| --- |
| For the pull up circuit shown in the figure, draw the pull down circuit and indicate the transistor ratios to guarantee a *worst-case* gate delay equal to that of the basic inverter.  **E**  **D**  **C**  **B**  **A** |

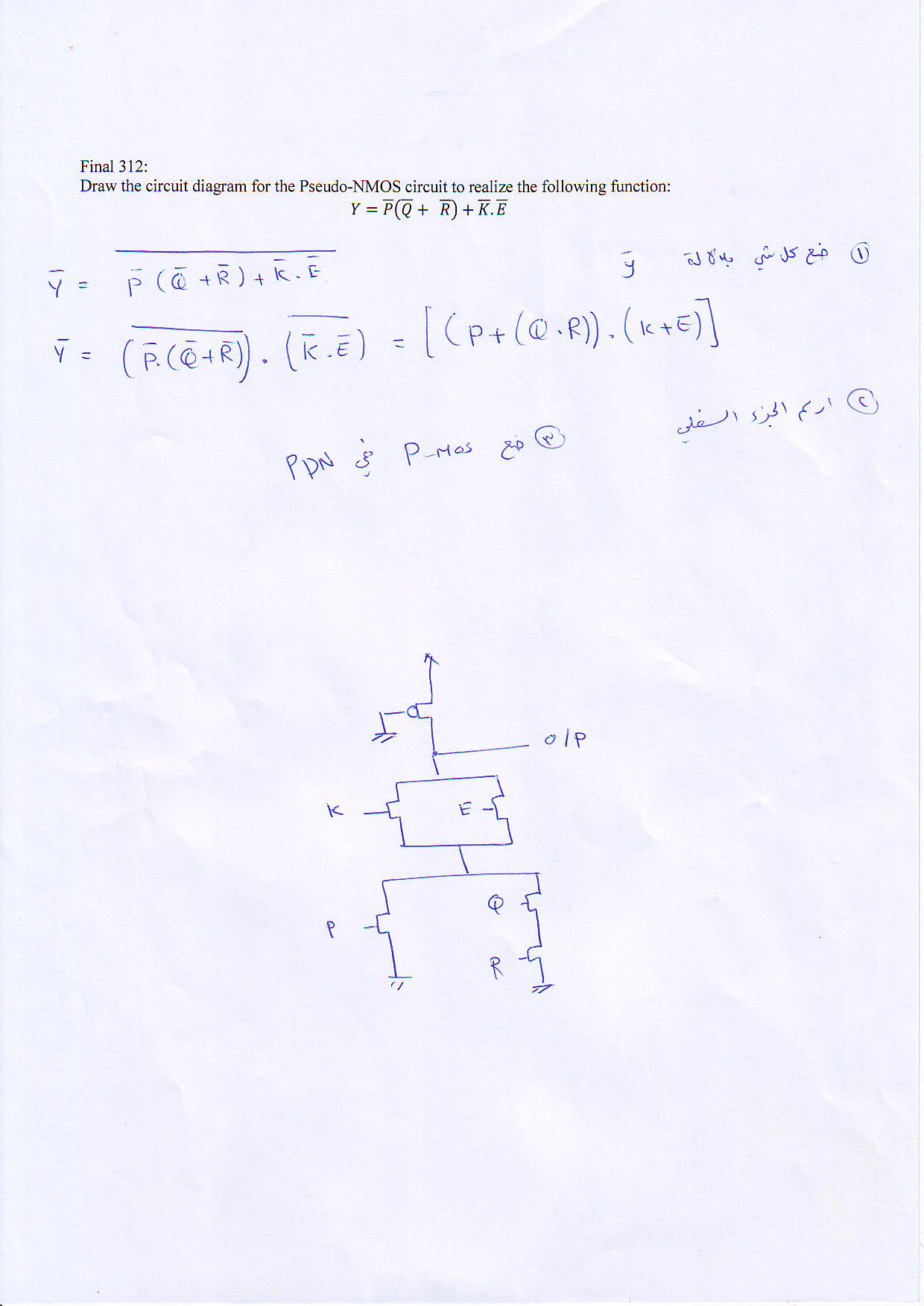


|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Find the operating regions for Qn and Qp transistors in a Pseudo-NMOS VTC. | |  |  |  |  |  | | --- | --- | --- | --- | --- | |  | region I | region II | region III | region IV | | Qn |  |  |  |  | | Qp |  |  |  |  | |
|  | |



Final 312:

Draw the circuit diagram for the Pseudo-NMOS circuit to realize the following function:



EE 401: Quiz

Name (Arabic): Student #

From the given CMOS Pull-down network:

1. Draw the Pull-up network
2. Size all transistors in the PUN and PDN to give matching delay to the basic CMOS inverter.

