King Saud University  
College of Engineering  
Electrical Engineering Department  

EE208: Logic Design  
(First Semester 1428/1429H)  

Second Mid-Term Exam  

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<tr>
<th>Instructors</th>
<th>Prof. A. Nouh, Dr. W. Gharieb, and Dr. Ridha AL Jamal</th>
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<tr>
<td>Date</td>
<td>MON, 30 Dhual-Qa’dah, 1428H (December 10, 2007)</td>
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<td>Time</td>
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<th>Question</th>
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الإجابة على نفس الورقة في المكان المخصص لكل سؤال

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<th>اسم الطالب</th>
<th>الرقم الجامعي</th>
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Question 1:
   a) Draw the internal circuit to implement a 3/8 decoder with enable input (3 Marks)

   b) Implement the following function using only one decoder 2/4 with inverted outputs.
       \[ F(a, b, c) = \sum m(1, 4, 5) \] (3 Marks)

Answer to question 1:
**Question 2:**

Let consider two multiplexers: the 74151 (Mux 8x1) and 74150 (Mux 16x1) as depicted in the following figure:

![Multiplexer Diagram](image)

**Answer to question 2:**

a/ Find the truth table of the multiplexer 16x1

b/ Construct this multiplexer using two multiplexers 74151

c/ Construct a 64x1 multiplexer using four 74150 16x1 multiplexers and one 74151 8x1 multiplexer. 

(7 Marks)
Question 3:

a) Use PLA with 3 inputs, 3 product terms, and 2 outputs to implement the following functions

\[ F_1(A, B, C, D) = \sum m(1, 2, 3, 8) + \sum d(0, 10, 12) \]
\[ F_2(A, B, C, D) = \sum m(0, 2, 8, 9, 10, 11, 13, 15) \]

Write only the program table

(4 Marks)

a) Compute the ROM size to implement the following function where X is a 3-bits input code and Y is the output code

\[ Y = 40 - (X-5)^2 \]

(3 Marks)

Answer to question 3: