

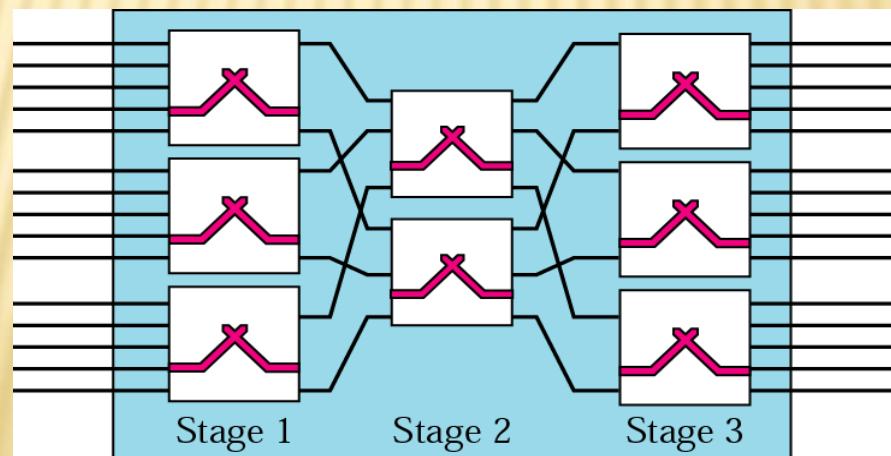
BROADBAND AND HIGH SPEED NETWORKS

2

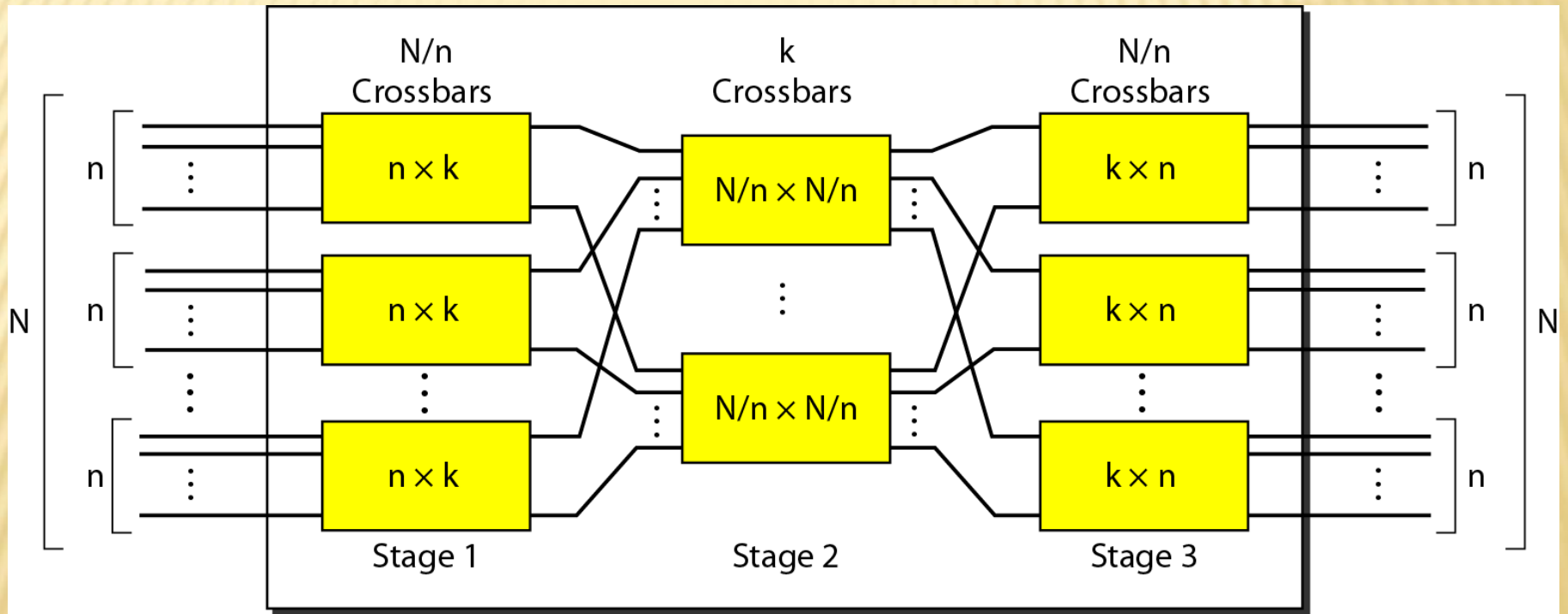
Switching

II - MULTISTAGE SWITCH

- ✘ Multistage switch combines crossbar switches in several stages.
- ✘ Design of a multistage switch depends on the number of stages and the number of switches required (or desired) in each stage.
- ✘ Normally, the middle stages have fewer switches than do the first and last stages.

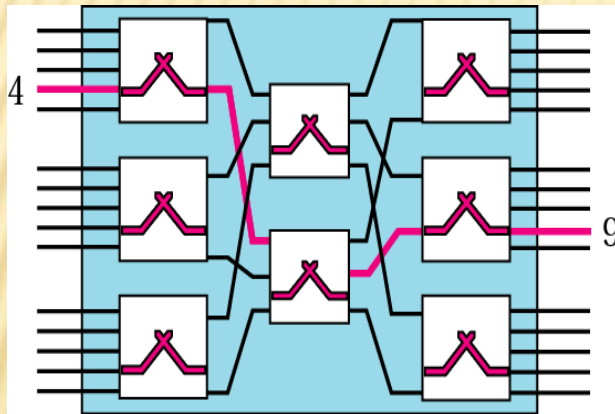


Multistage switch

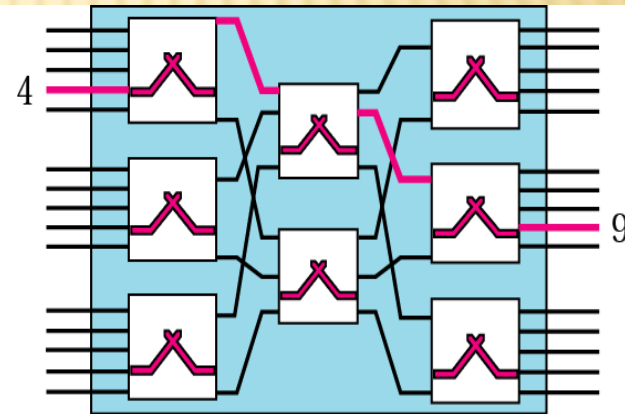


MULTIPLE SWITCHING PATHS

- ✘ Multiple paths are available in multistage switches.
- ✘ Blocking refers to times when two inputs are looking for the same output. The output port is blocked.

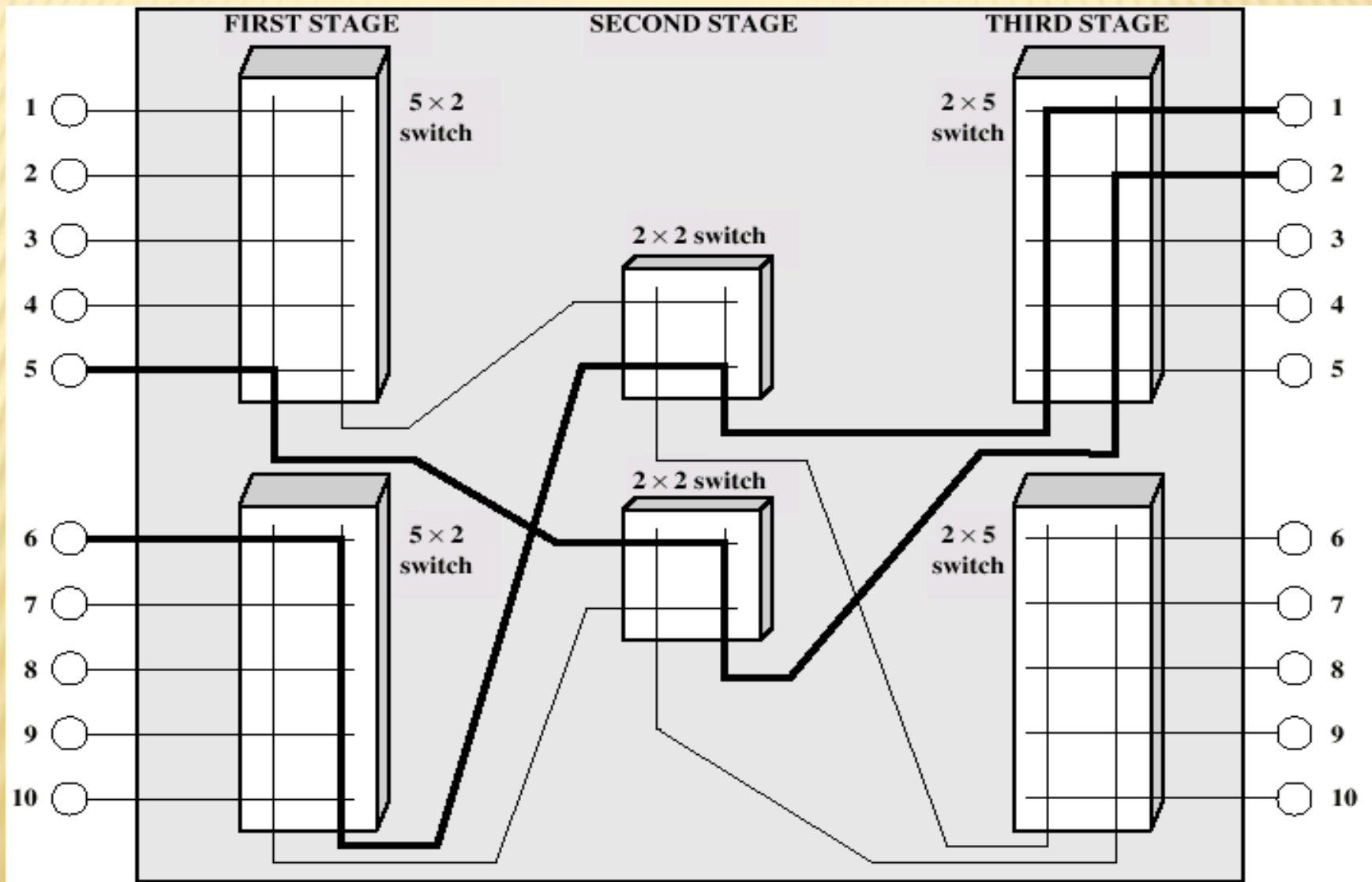


a. First option



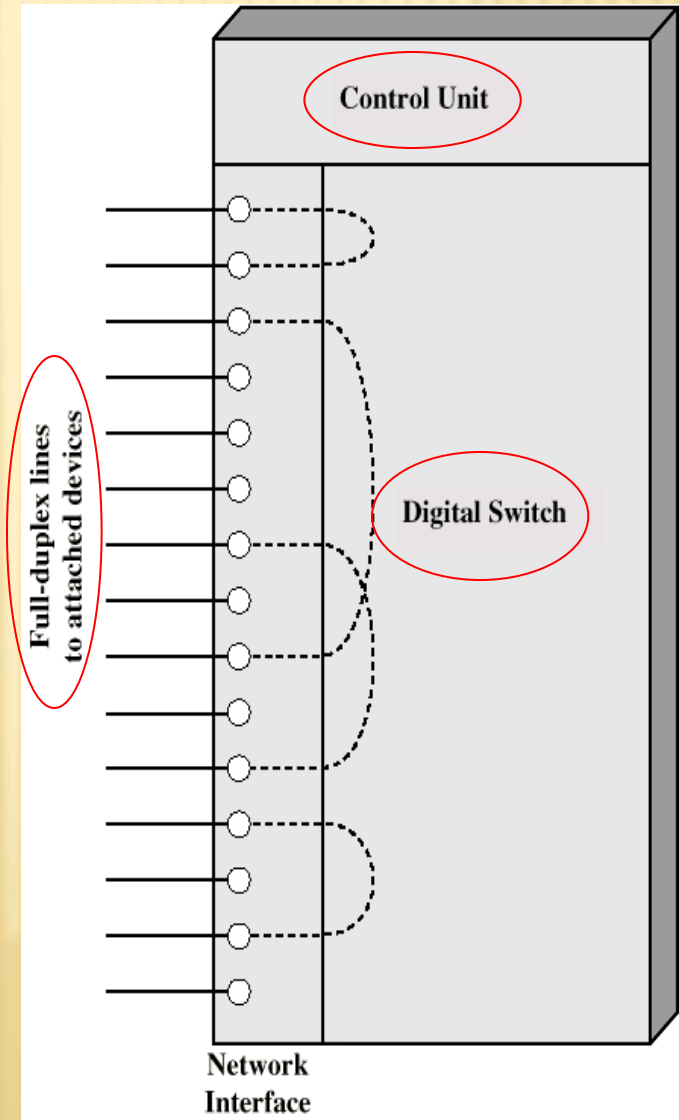
b. Second option

THREE STAGES SWITCH



CIRCUIT SWITCH CONCEPTS & ELEMENTS

- Digital Switch
 - Provide transparent signal path between devices
- Network Interface
- Control Unit
 - Establish connections
 - Generally on demand
 - Handle and acknowledge requests
 - Determine if destination is free
 - construct path
 - Maintain connection
 - Disconnect



DIGITAL SWITCH: BLOCKING VS. NON-BLOCKING

- **Blocking**

- A network is unable to connect end stations because all paths are in use
- Used on voice systems
 - Short duration calls

- **Non-blocking**

- Permits all stations to connect (in pairs) at once
- Used for some data connections

II. Multistage Interconnection Networks (MINs):

Characteristics:

1. Full Access:

- ❖ Every input link can reach to any output link in a single pass.
- ❖ In MINs, by using 2×2 switching elements, only $\log_2 N$ stages are required to achieve *full access capability*.

2. Strictly Non-Blocking vs. Internal Blocking:

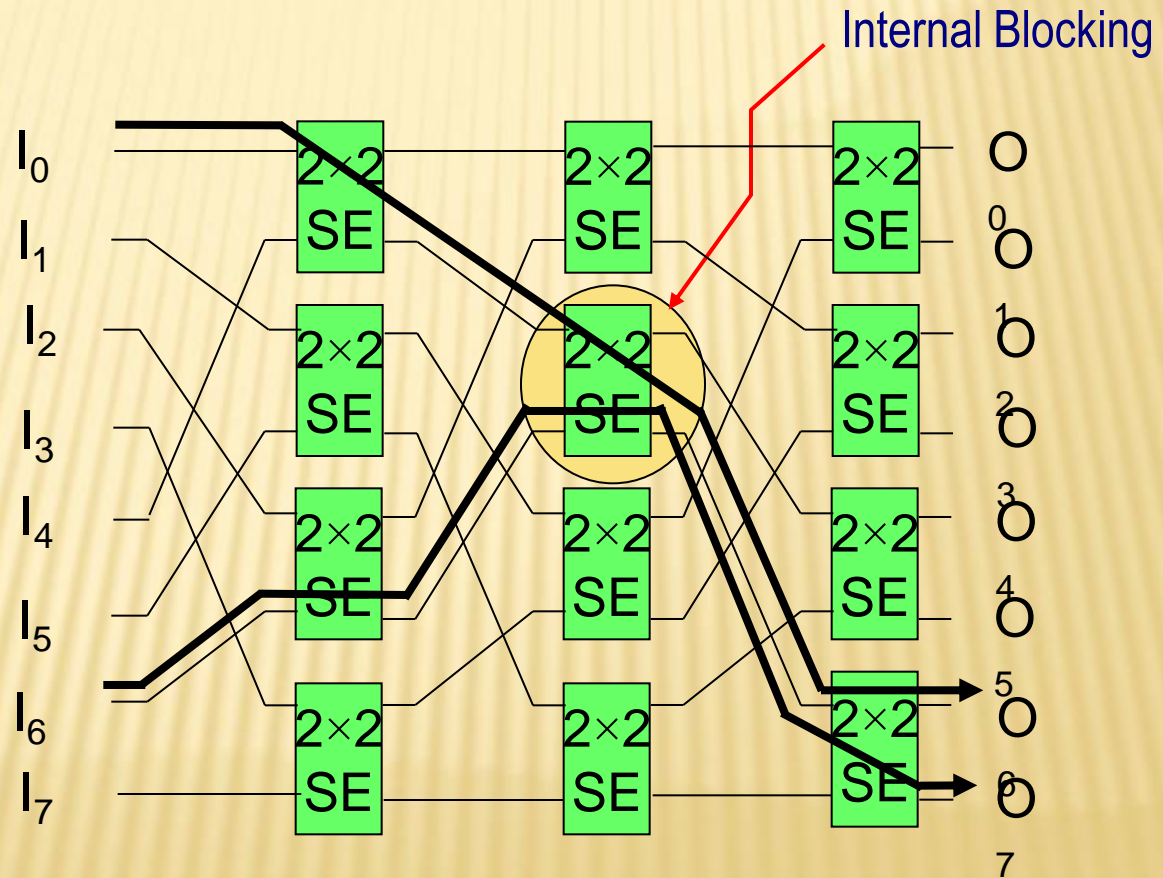
- ❖ **Strictly non-blocking Switch** can realize $N!$ permutations without any rearrangement of the existing connections.
- ❖ MINs with fewer stages suffer problem **of internal blocking**.

INTERNAL BLOCKING IN (MIN)

Internal Blocking occurs for the connections:

0 → 6

6 → 7



3. Rearrangeable Networks:

- ❖ MINs are capable to realize $N!$ permutations by choosing the appropriate connections.
- ❖ This type of MINs requires a large number of stages ($3\log_2 N - 4$).

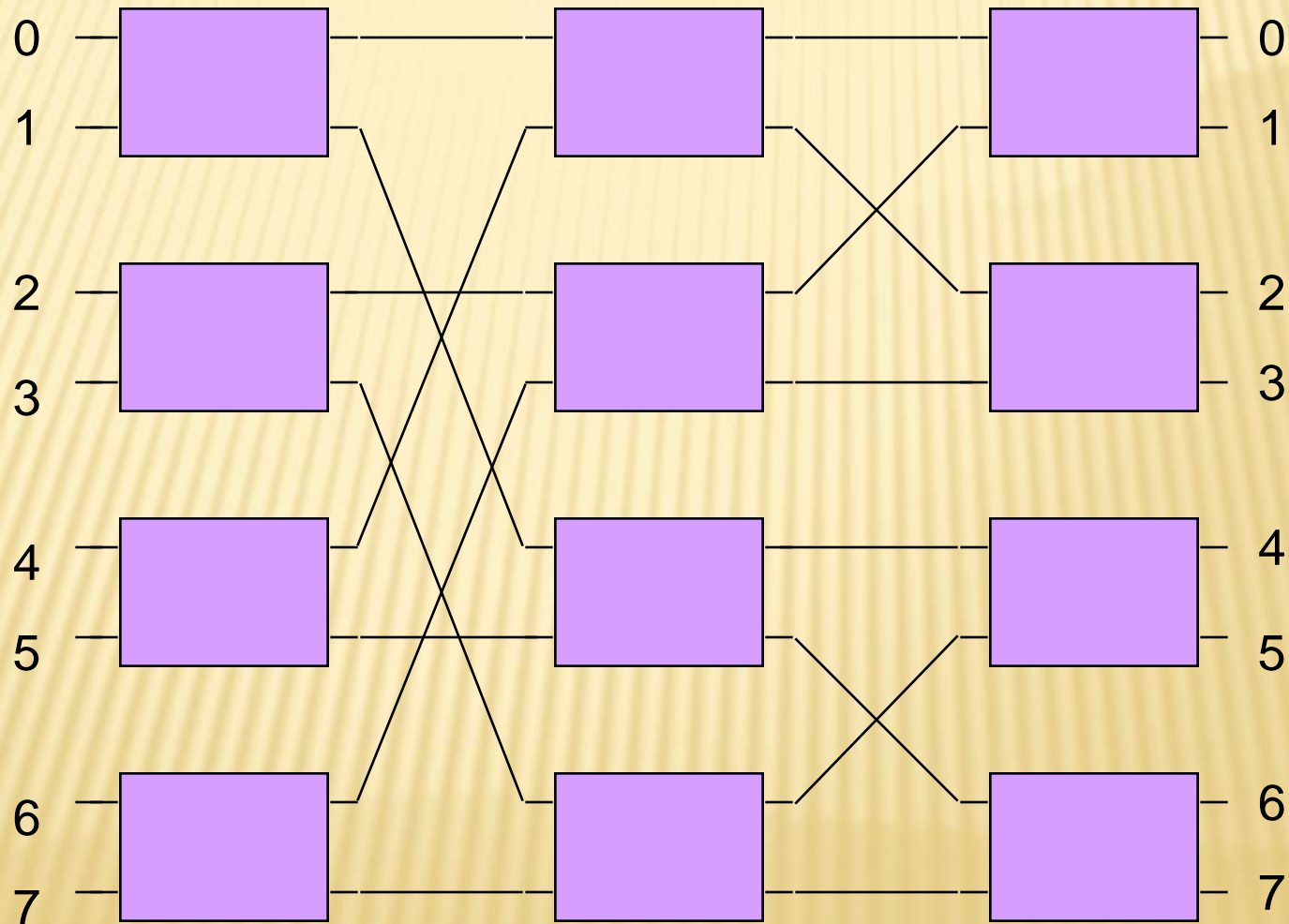
4. Combinatorial Power:

- ❖ It is the ratio of the number of permutations realizable by the MINs to the total number of possible permutations ($N!$).
- ❖ A MIN has $\log_2 N$ stages are required to achieve full access capability, and in each stage, there are $N/2$ of 2×2 switching elements.
- ❖ Since each switching element has two configurations, namely straight and exchange, therefore, number of permutations realizable by the MINs is $2^{N/2 \cdot \log_2 N}$.

DELTA NETWORK

- The delta network is one example of a multistage interconnection network (Banyan Network) that can be used as a switch fabric.
- In banyan networks, there is a single path from each input port to each output port.

8 X 8 DELTA NETWORK

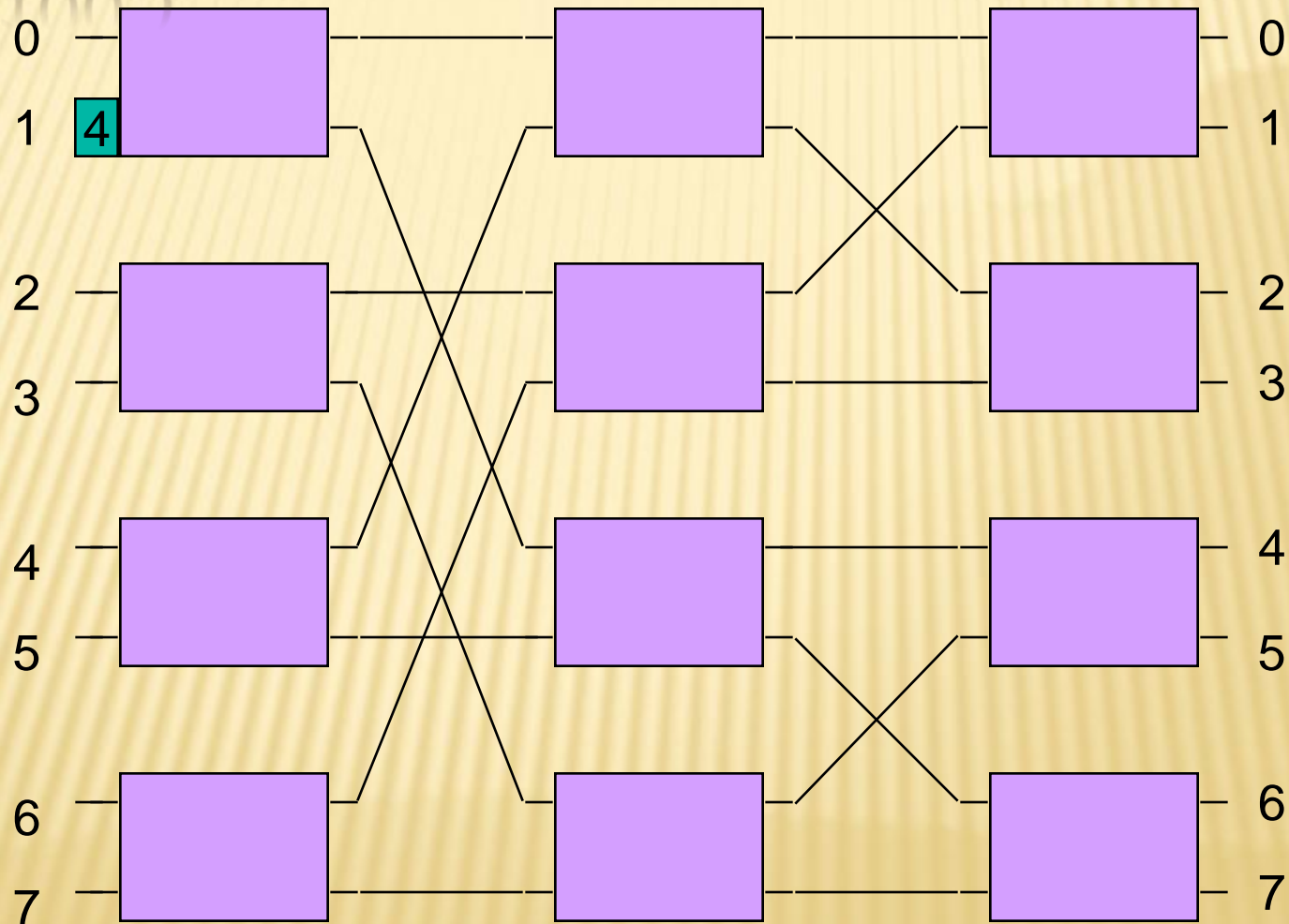


SELF ROUTING

- Delta network has self-routing property
- The path for a cell to reach its destination can be determined directly from its routing tag (i.e., destination port id)
- Stage k of the MIN looks at bit k of the tag
- If bit k is 0, then send cell out upper port
- If bit k is 1, then send cell out lower port

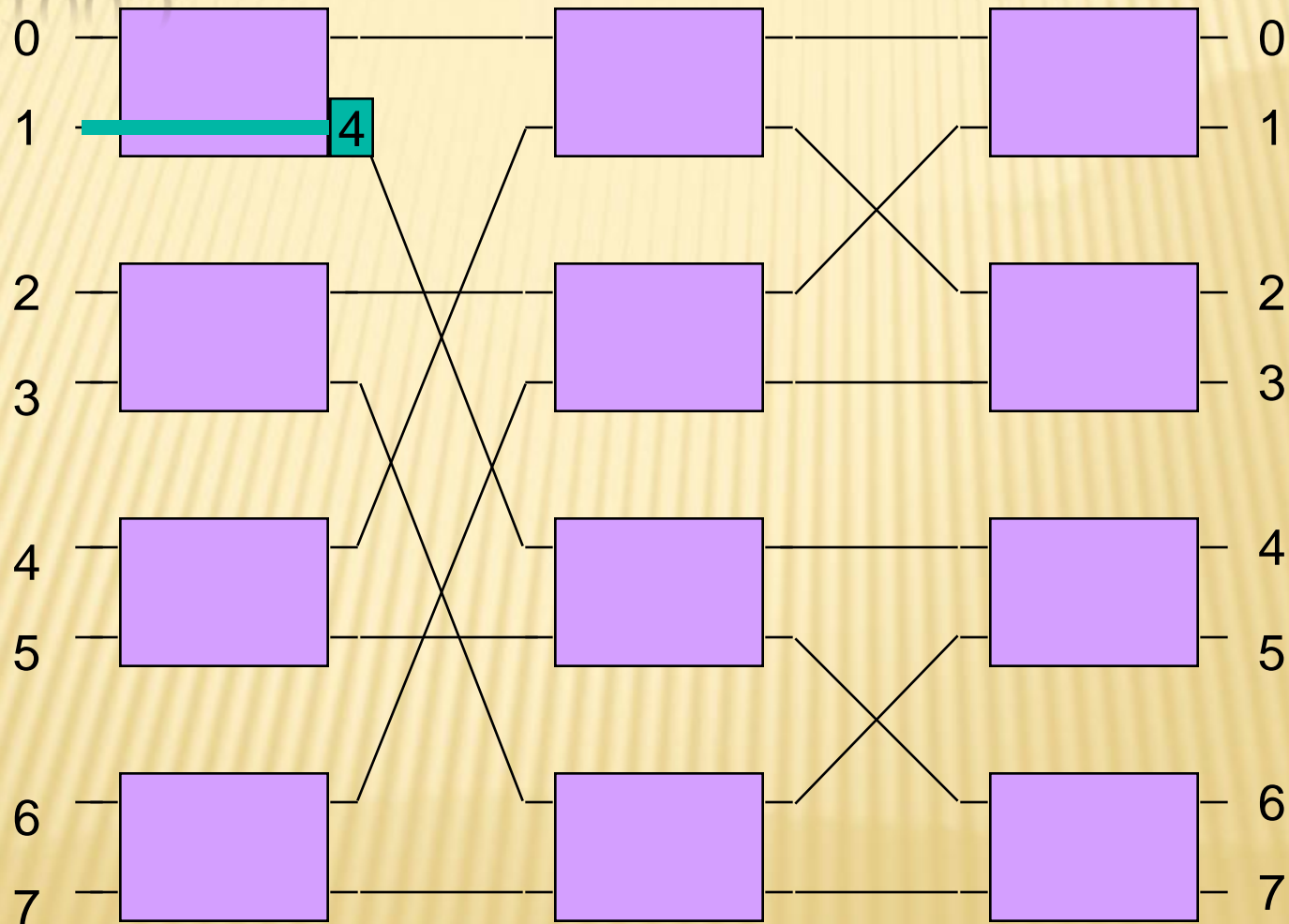
EXAMPLE OF SELF ROUTING CELL DESTINED FOR OUTPUT PORT 4 (= 100)

2



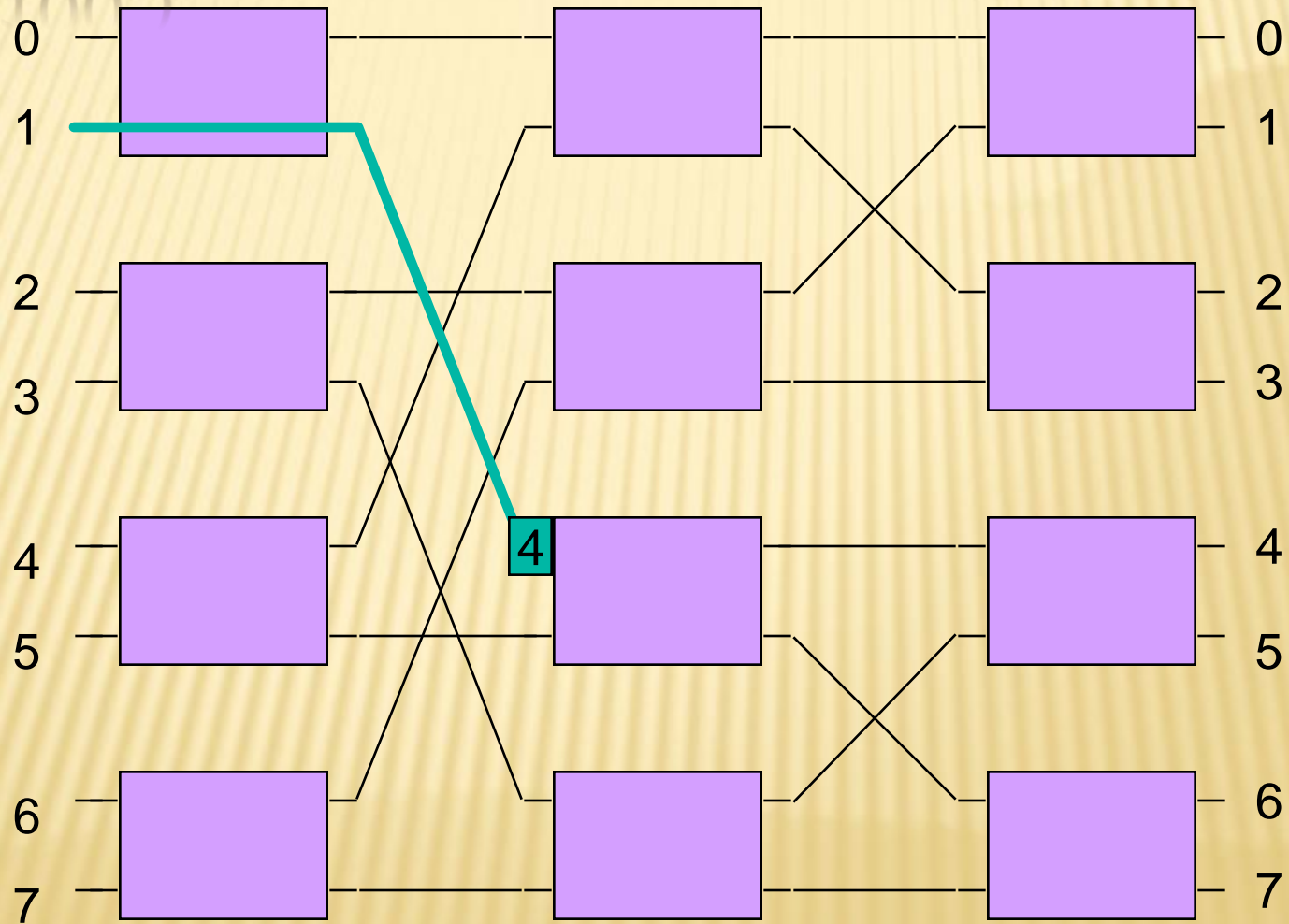
EXAMPLE OF SELF ROUTING CELL DESTINED FOR OUTPUT PORT 4 (= 100)

2



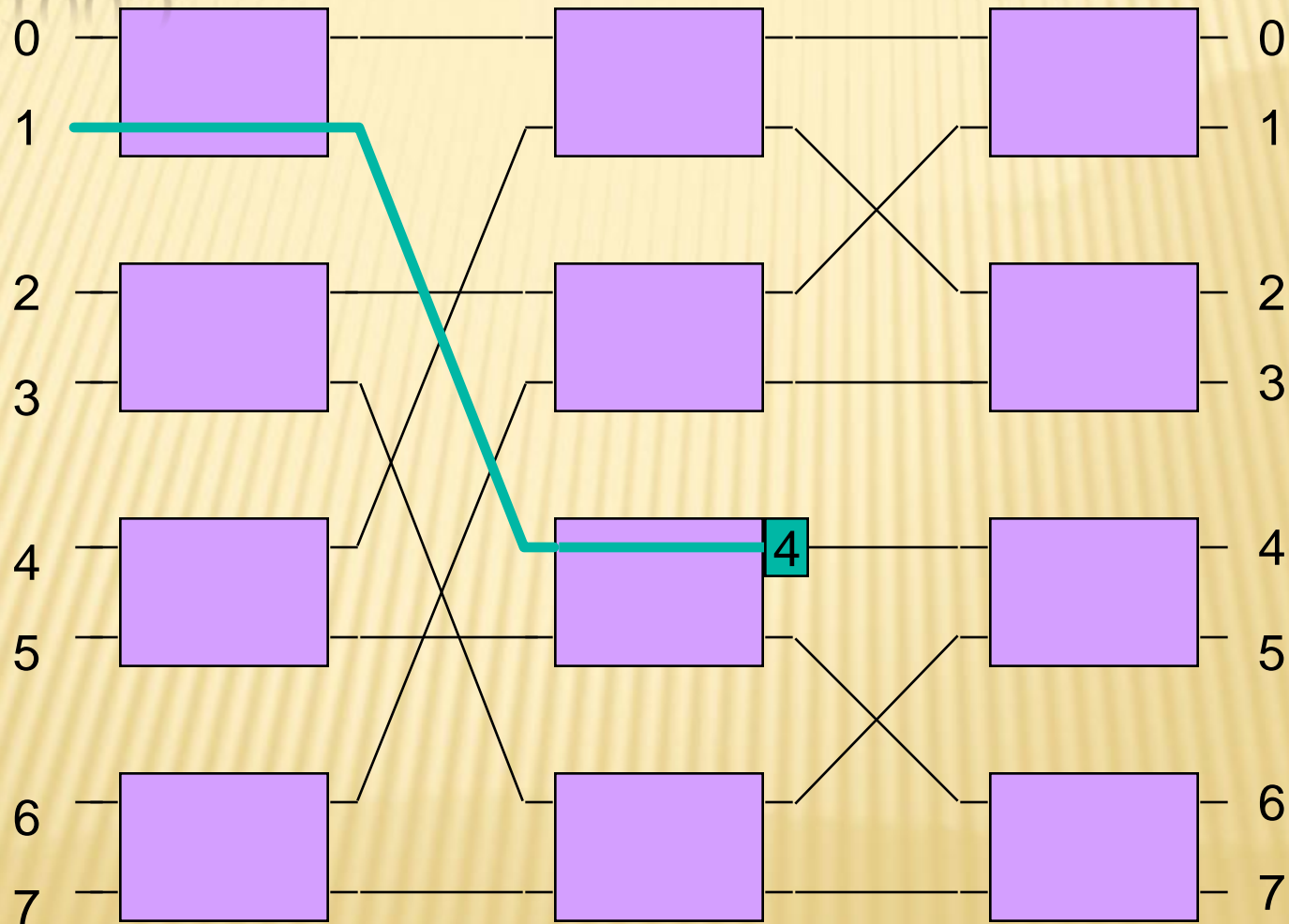
EXAMPLE OF SELF ROUTING CELL DESTINED FOR OUTPUT PORT 4 (= 100)

2



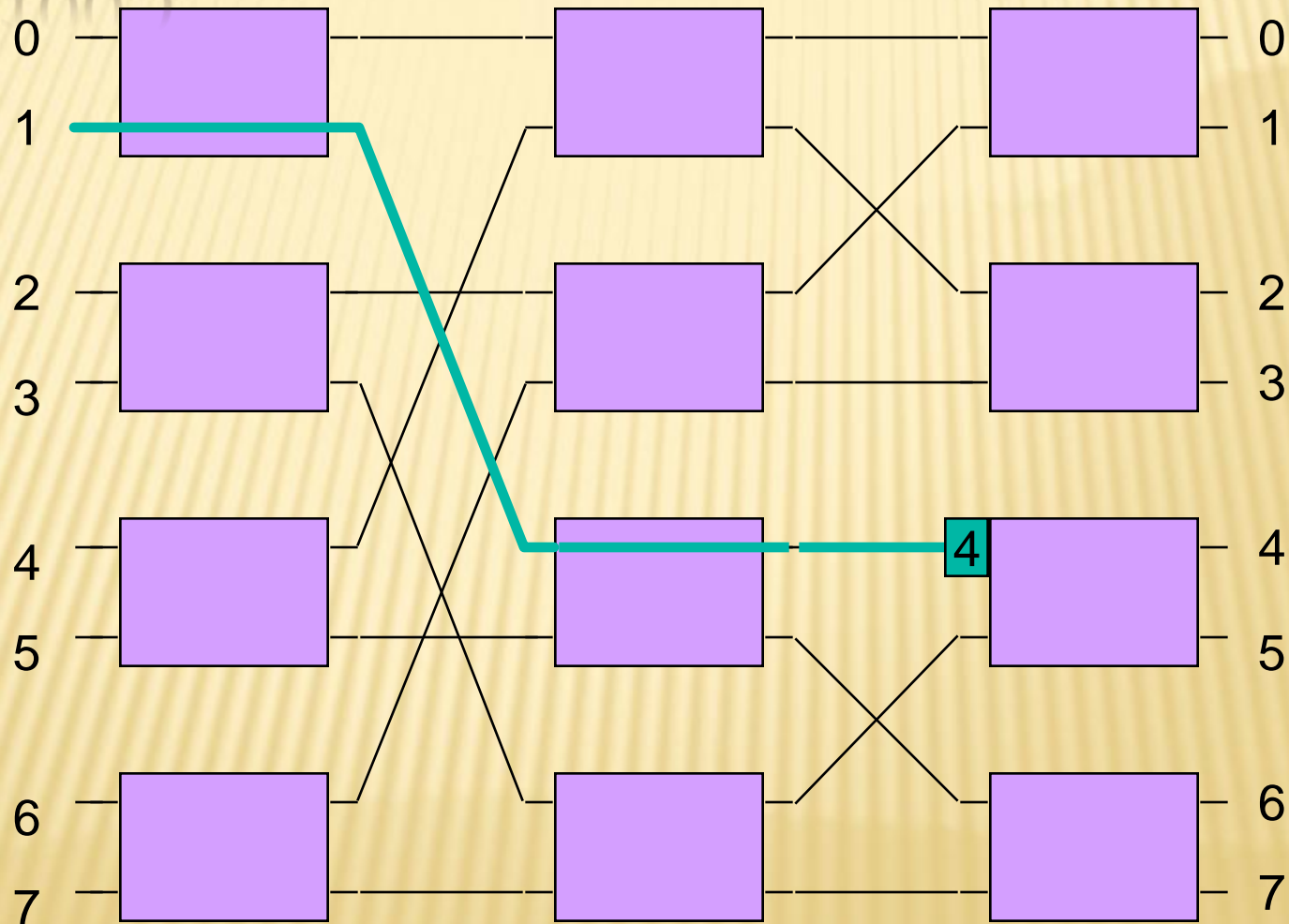
EXAMPLE OF SELF ROUTING CELL DESTINED FOR OUTPUT PORT 4 (= 100)

2



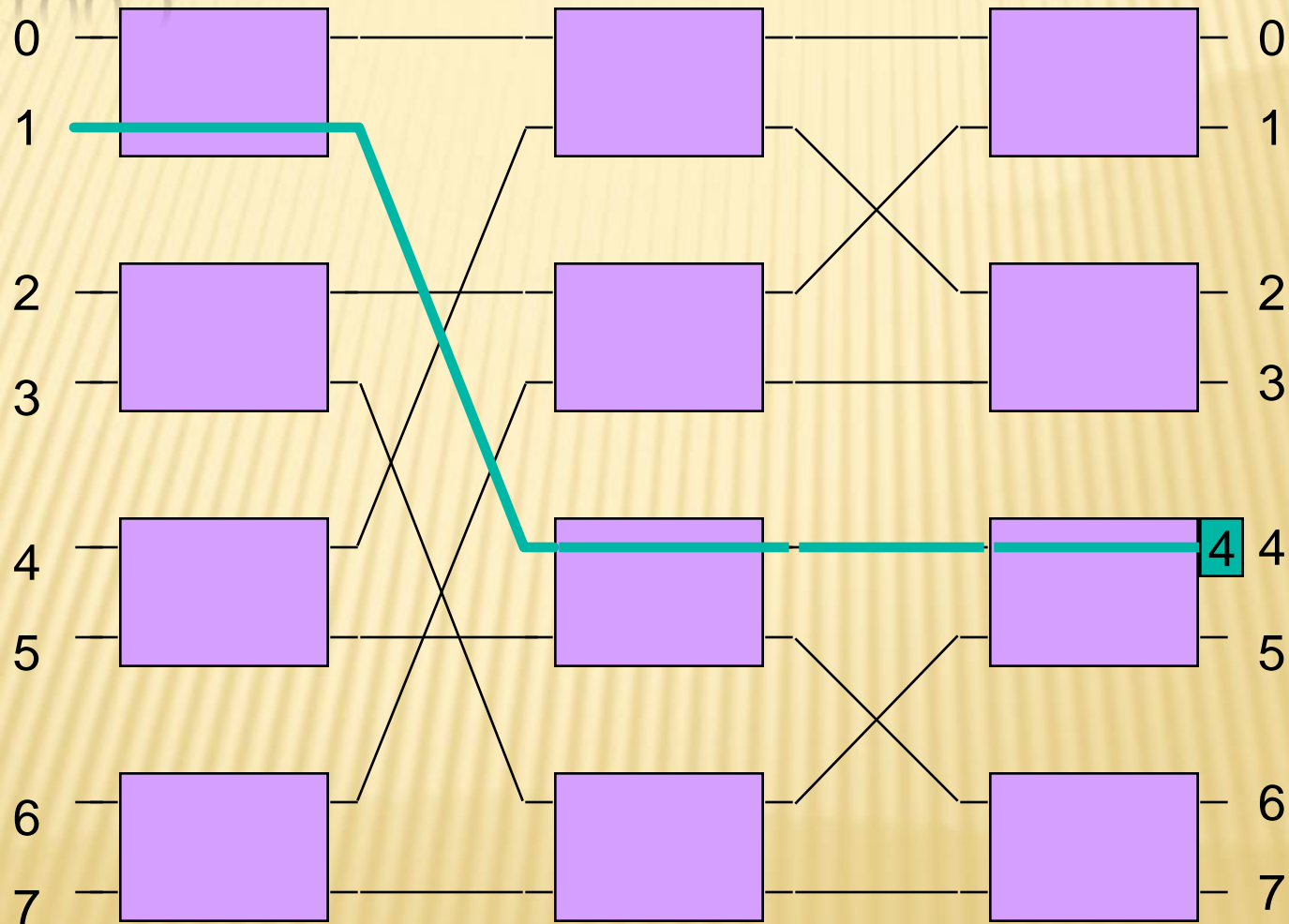
EXAMPLE OF SELF ROUTING CELL DESTINED FOR OUTPUT PORT 4 (= 100)

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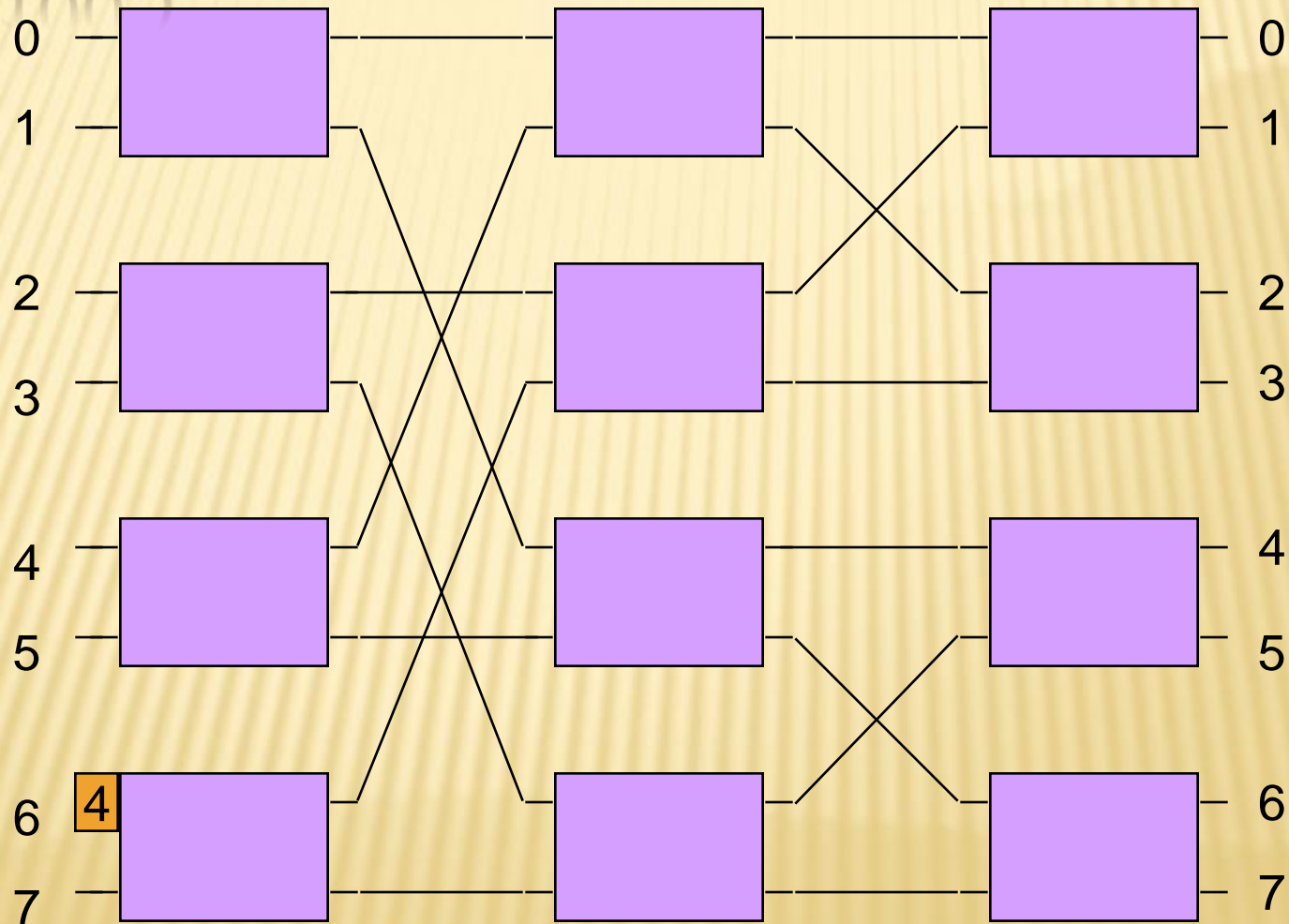
EXAMPLE OF SELF ROUTING CELL DESTINED FOR OUTPUT PORT 4 (= 100)

2



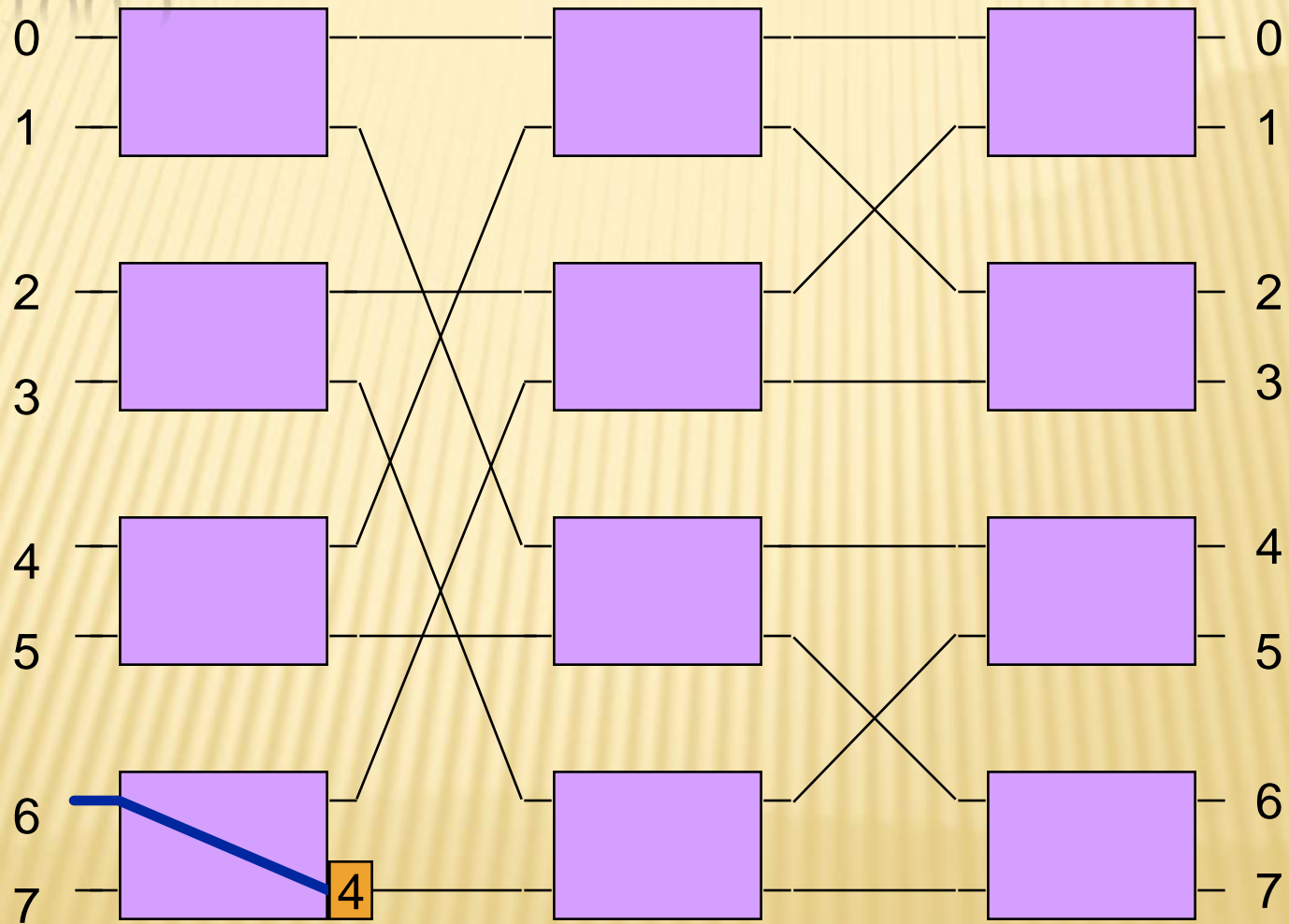
EXAMPLE OF SELF ROUTING CELL DESTINED FOR OUTPUT PORT 4 (= 100)

2



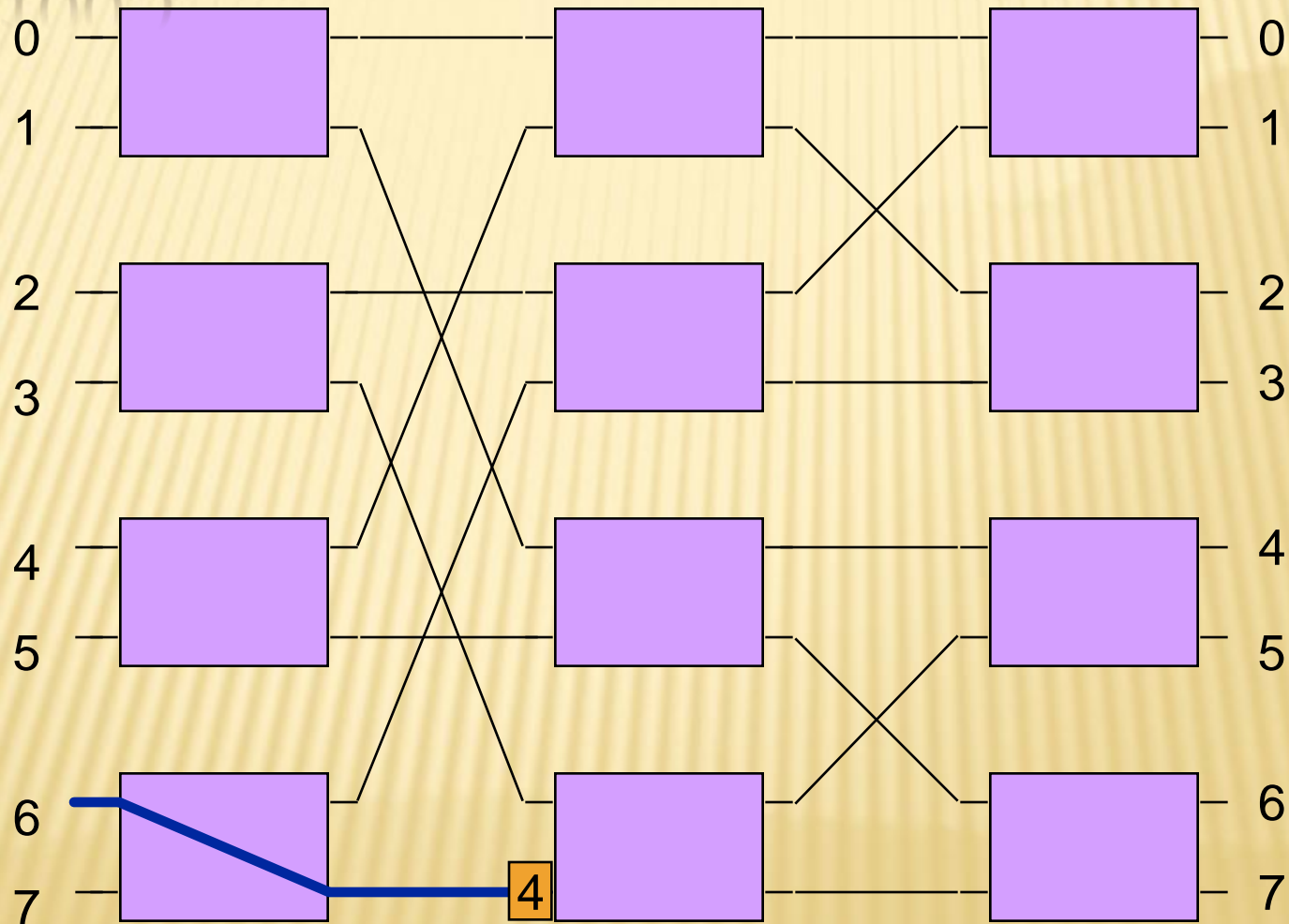
EXAMPLE OF SELF ROUTING CELL DESTINED FOR OUTPUT PORT 4 (= 100)

2



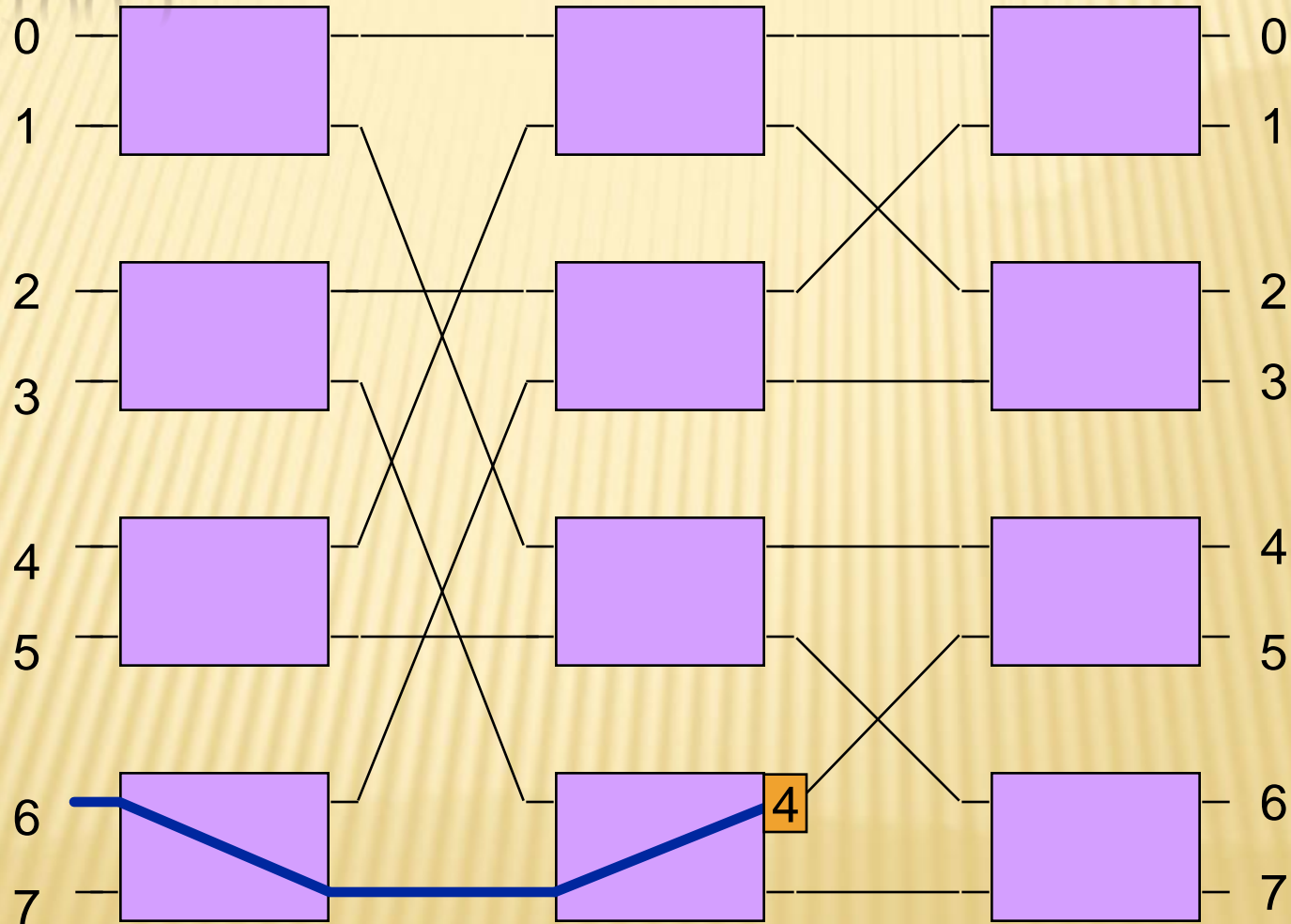
EXAMPLE OF SELF ROUTING CELL DESTINED FOR OUTPUT PORT 4 (= 100)

2



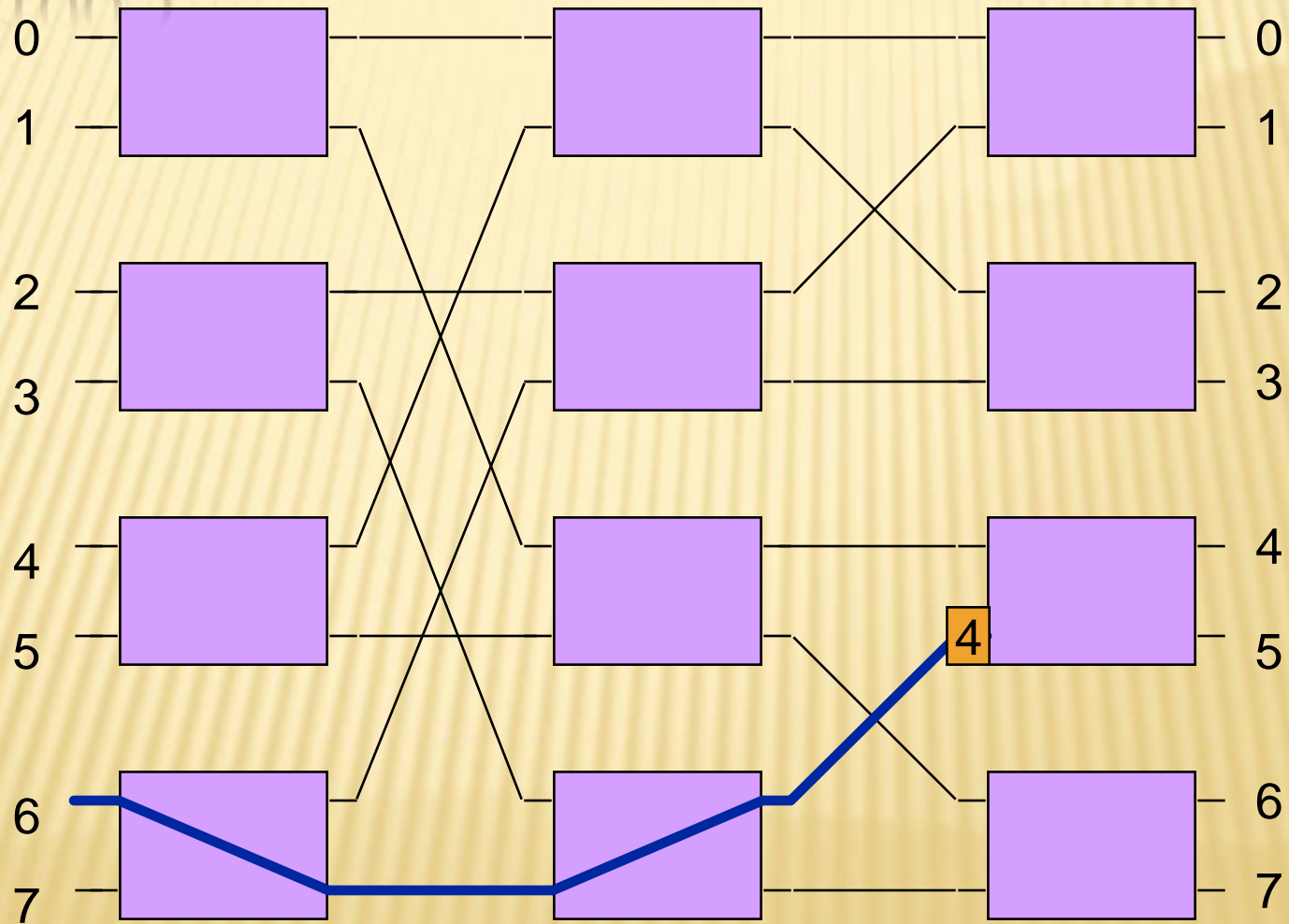
EXAMPLE OF SELF ROUTING CELL DESTINED FOR OUTPUT PORT 4 (= 100)

2



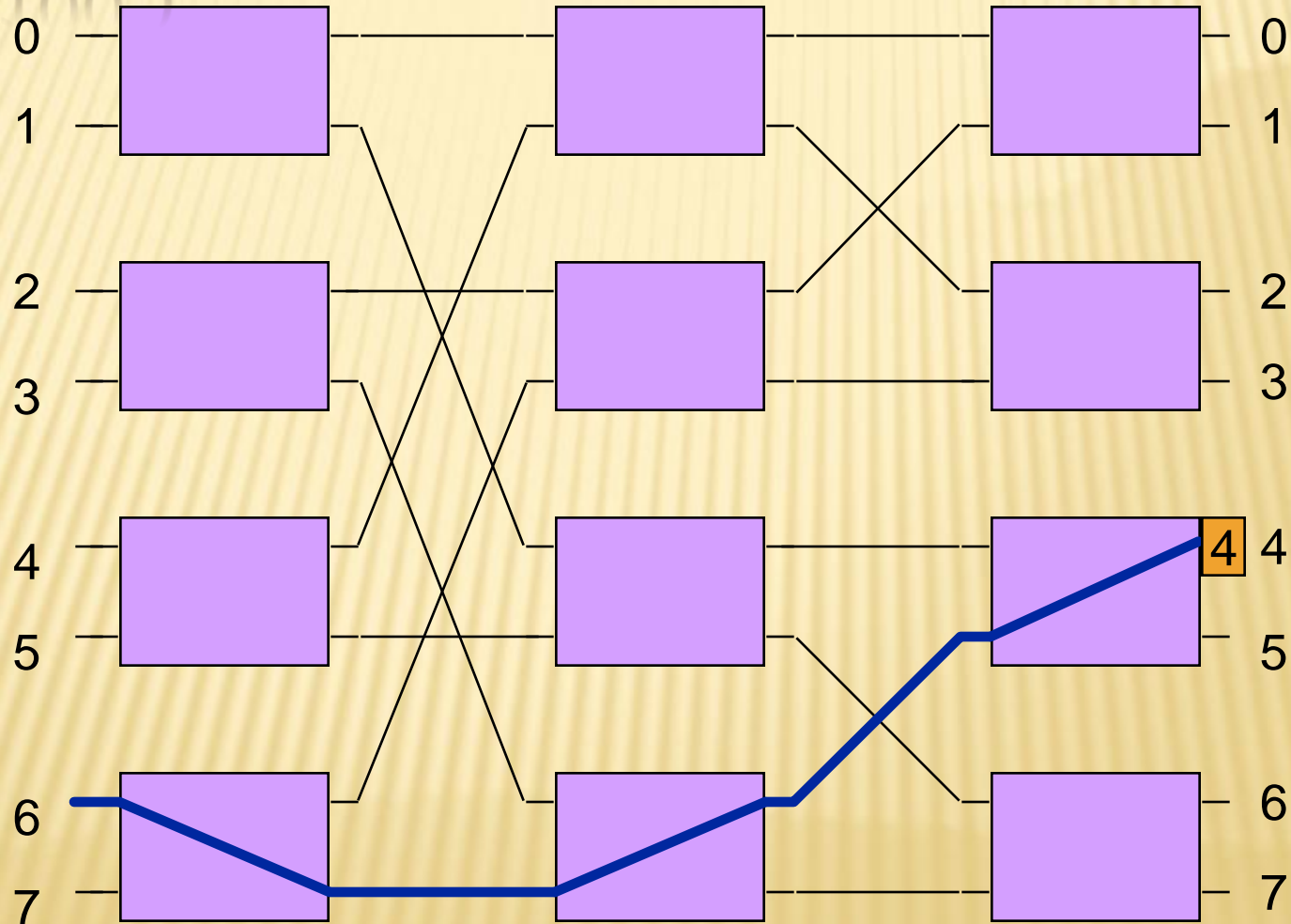
EXAMPLE OF SELF ROUTING CELL DESTINED FOR OUTPUT PORT 4 (= 100)

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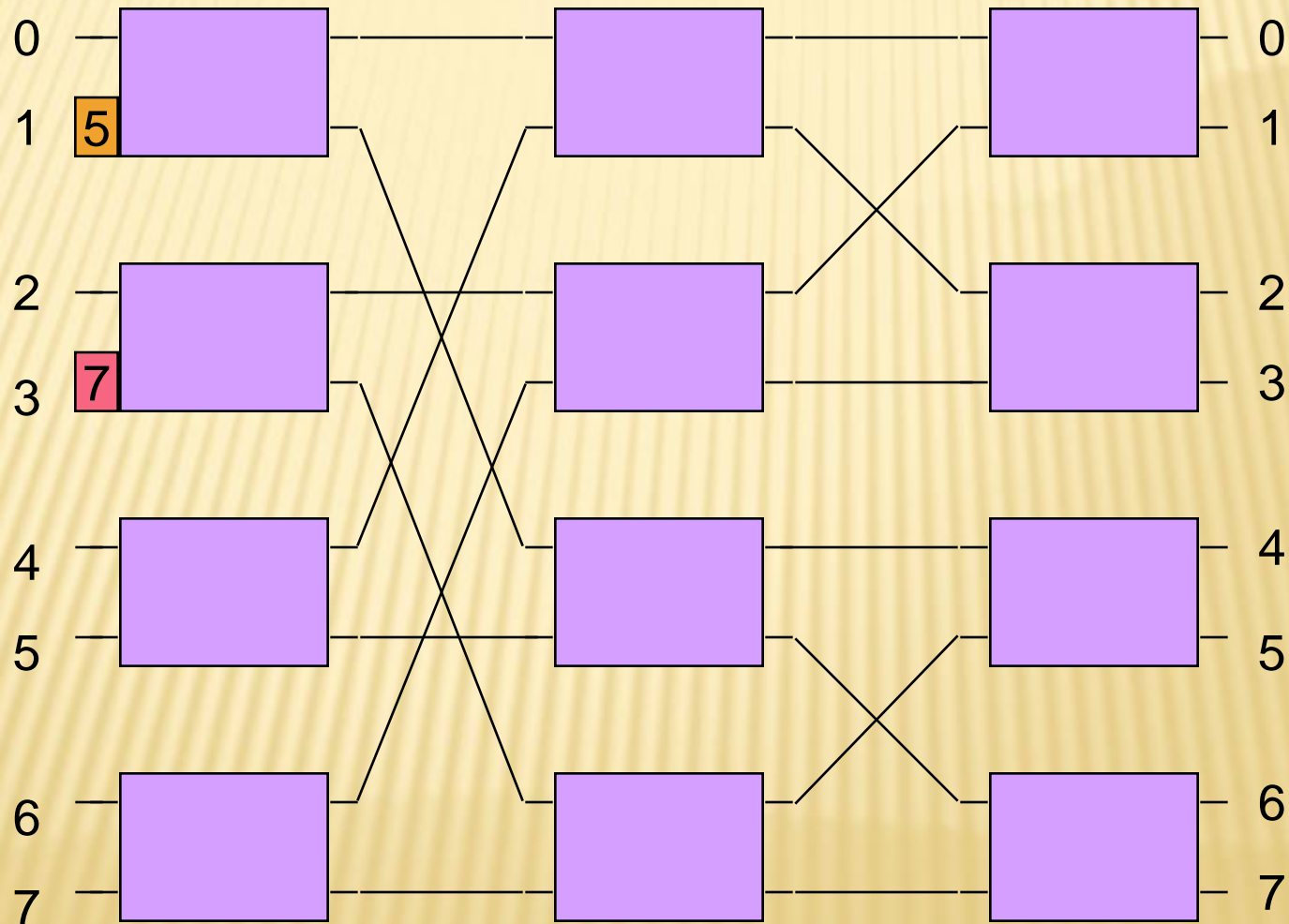


EXAMPLE OF SELF ROUTING CELL DESTINED FOR OUTPUT PORT 4 (= 100)

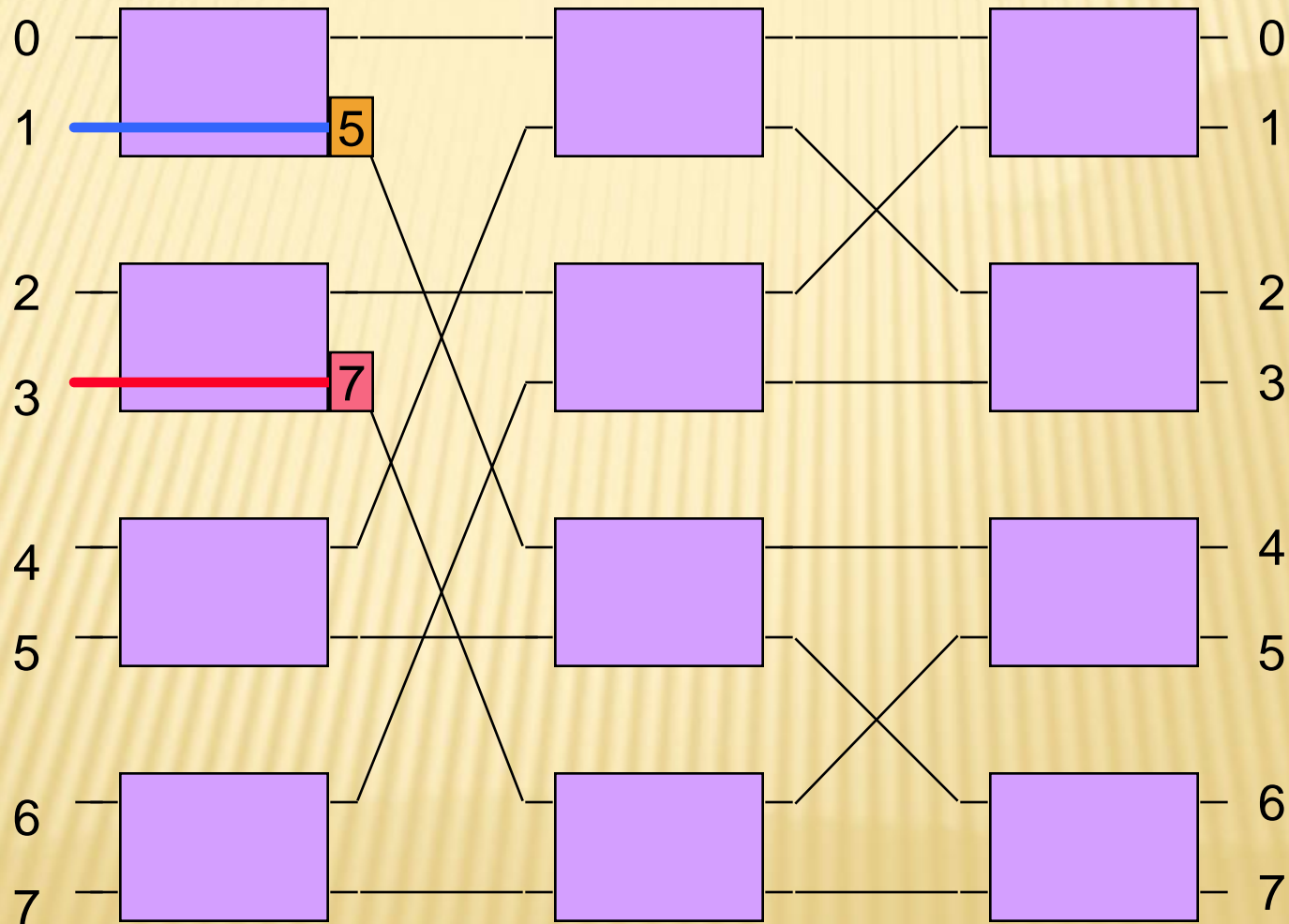
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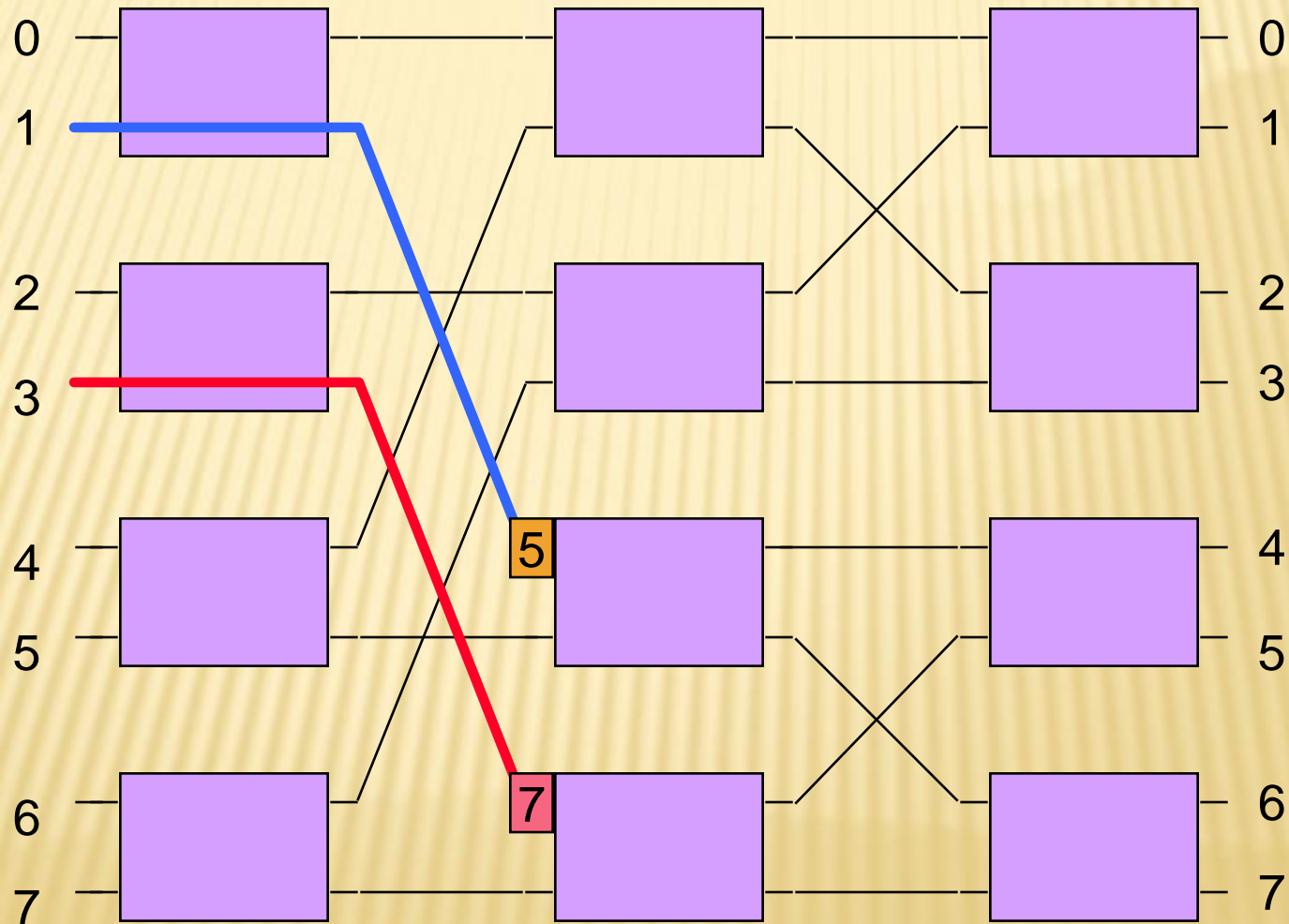
MULTIPLE CONCURRENT PATHS



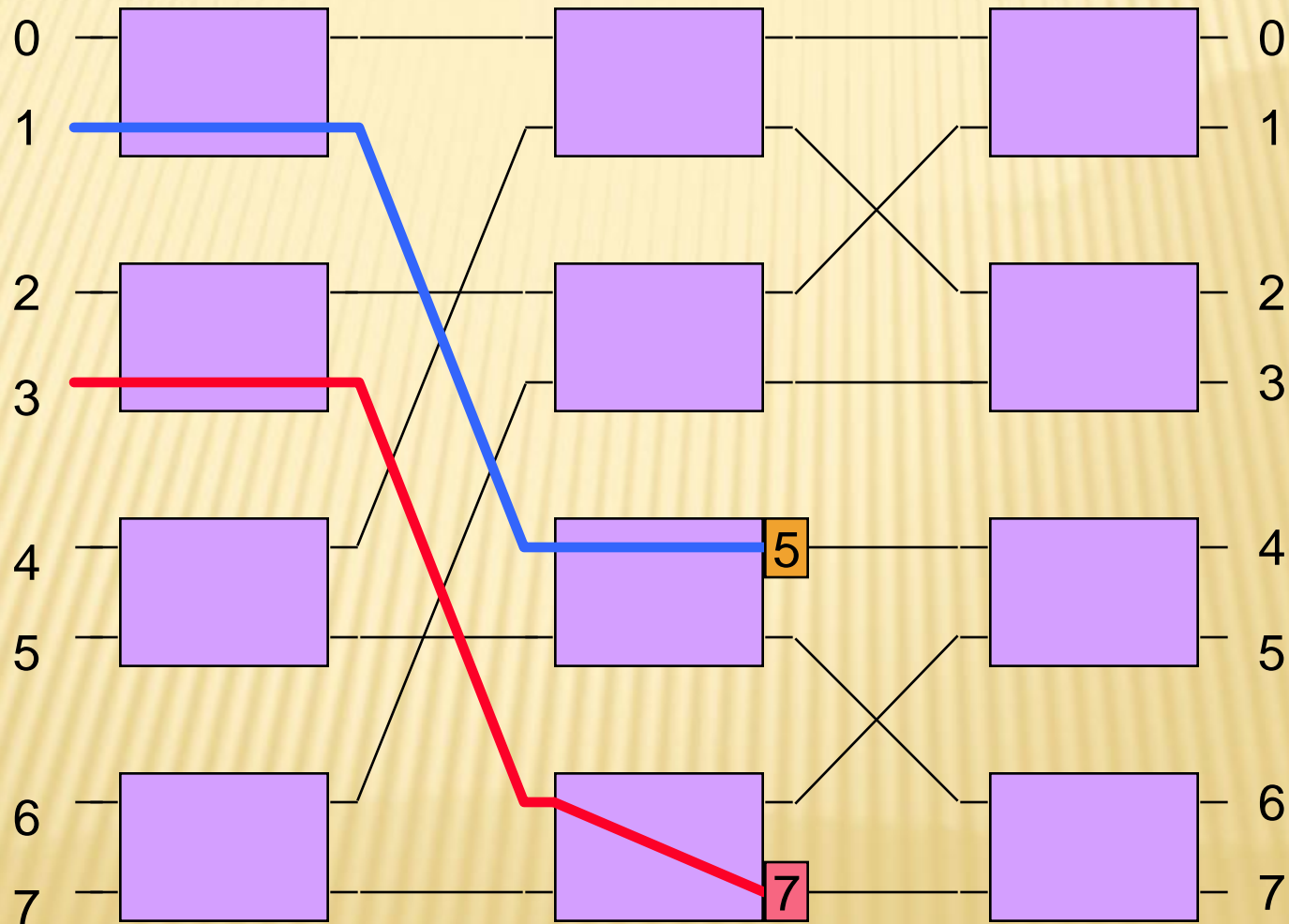
MULTIPLE CONCURRENT PATHS



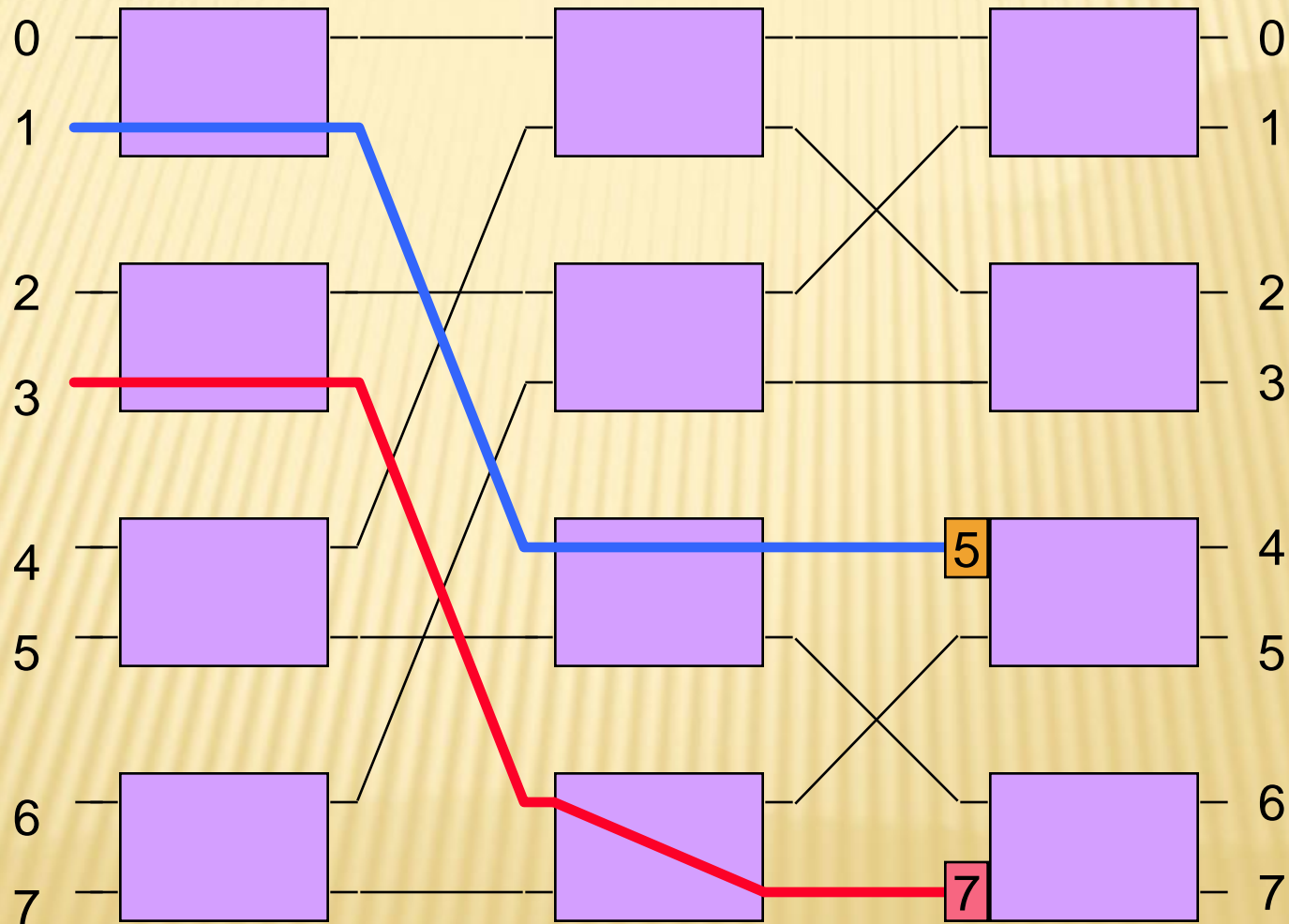
MULTIPLE CONCURRENT PATHS



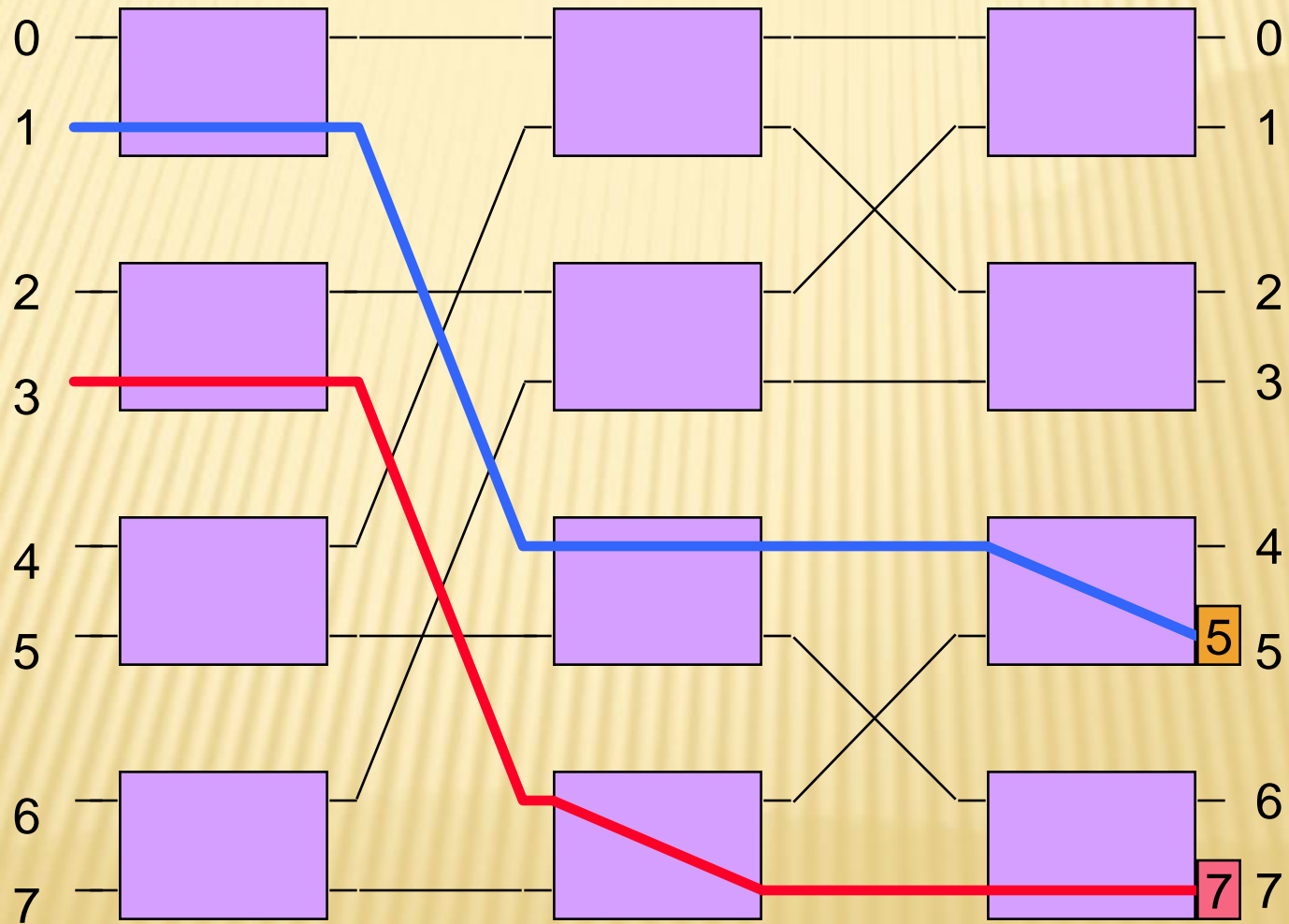
MULTIPLE CONCURRENT PATHS



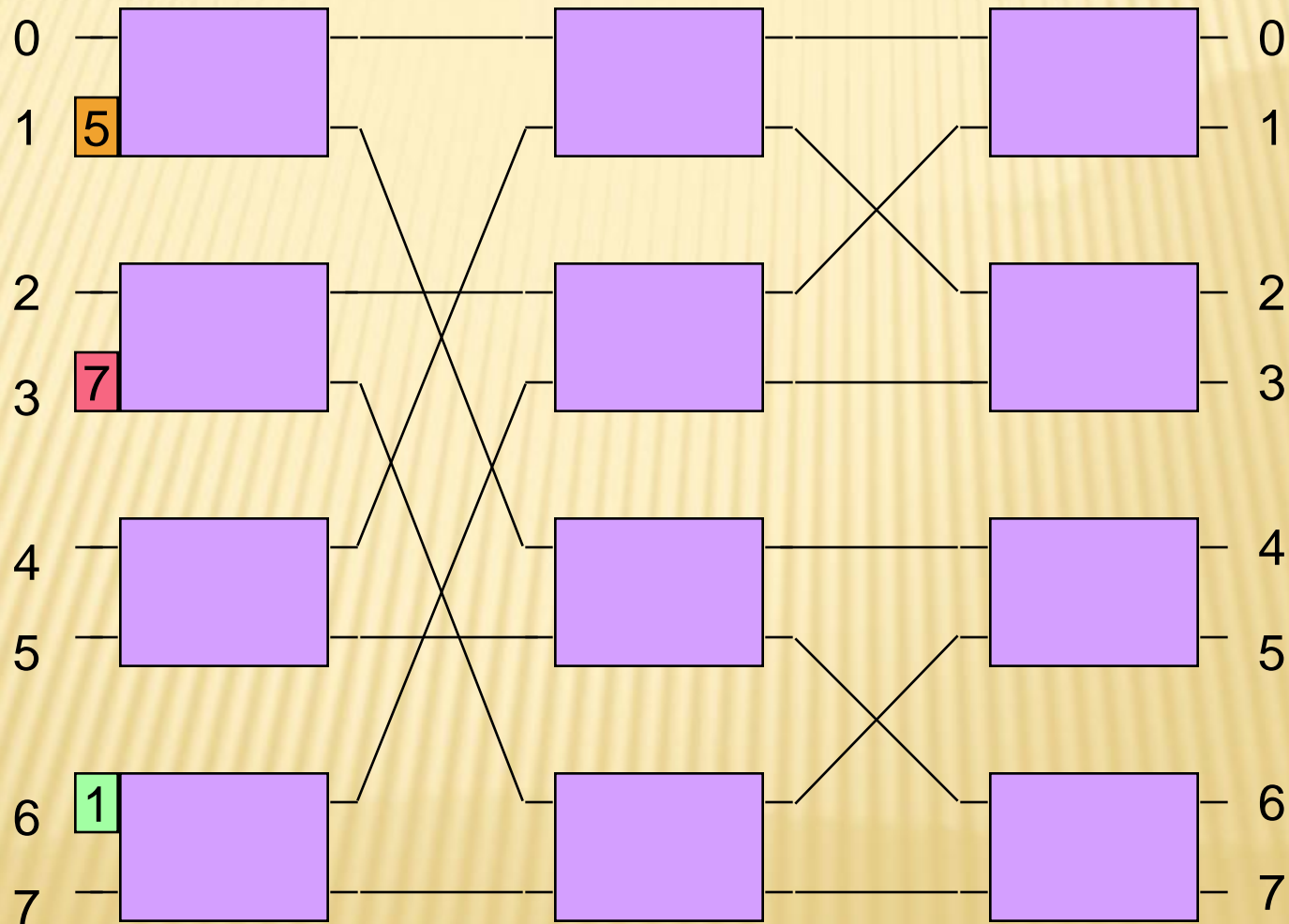
MULTIPLE CONCURRENT PATHS



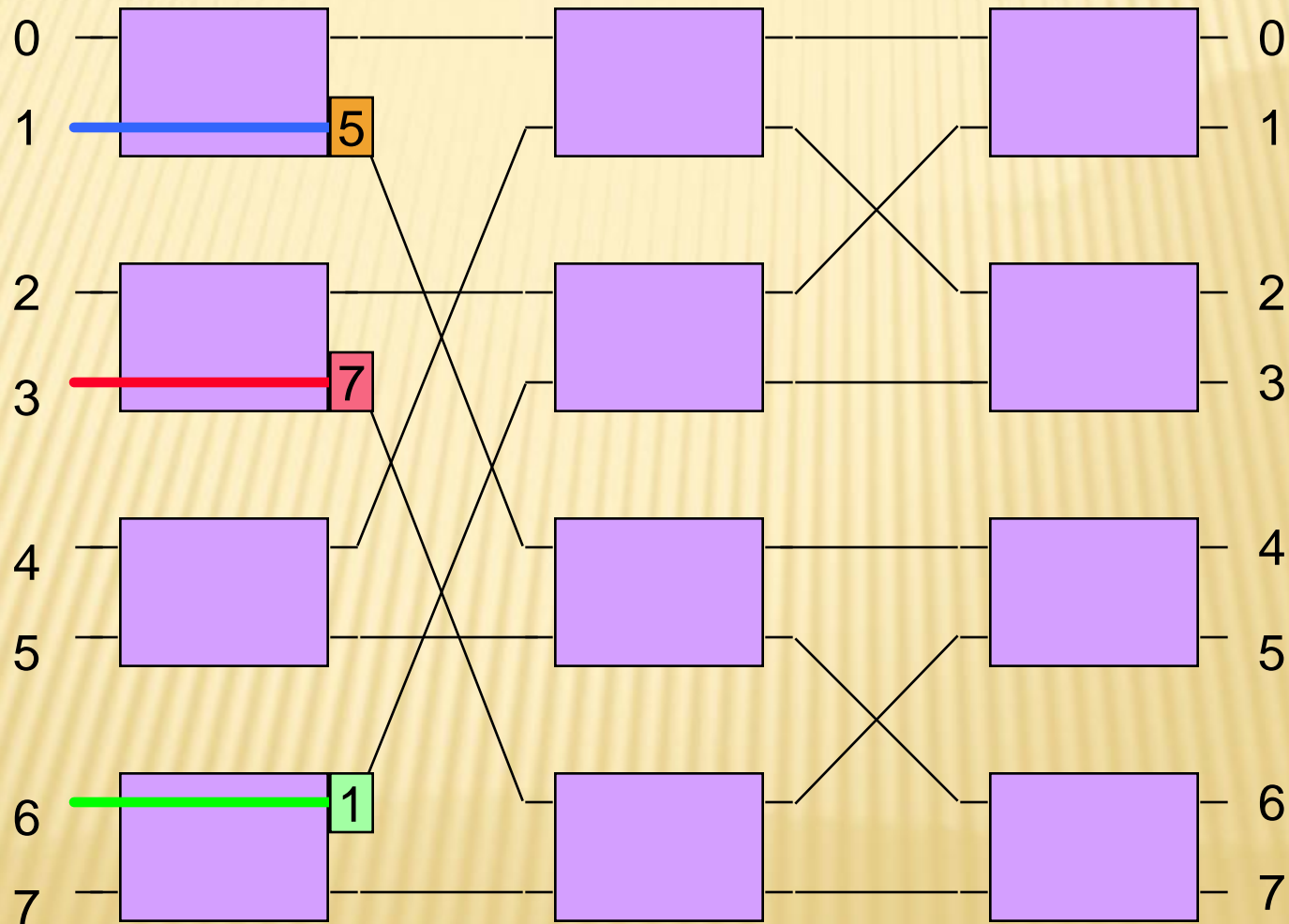
MULTIPLE CONCURRENT PATHS



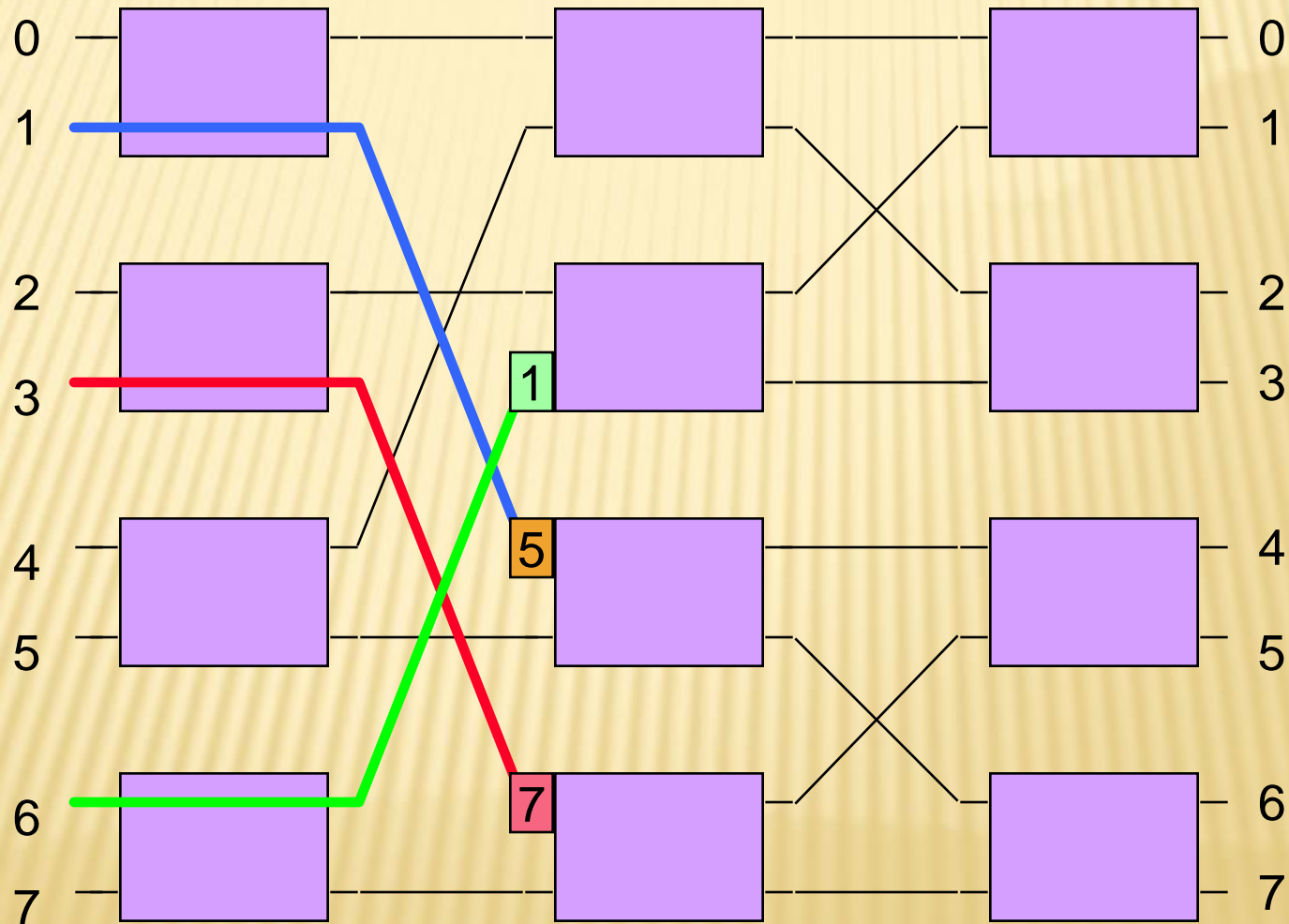
MULTIPLE CONCURRENT PATHS



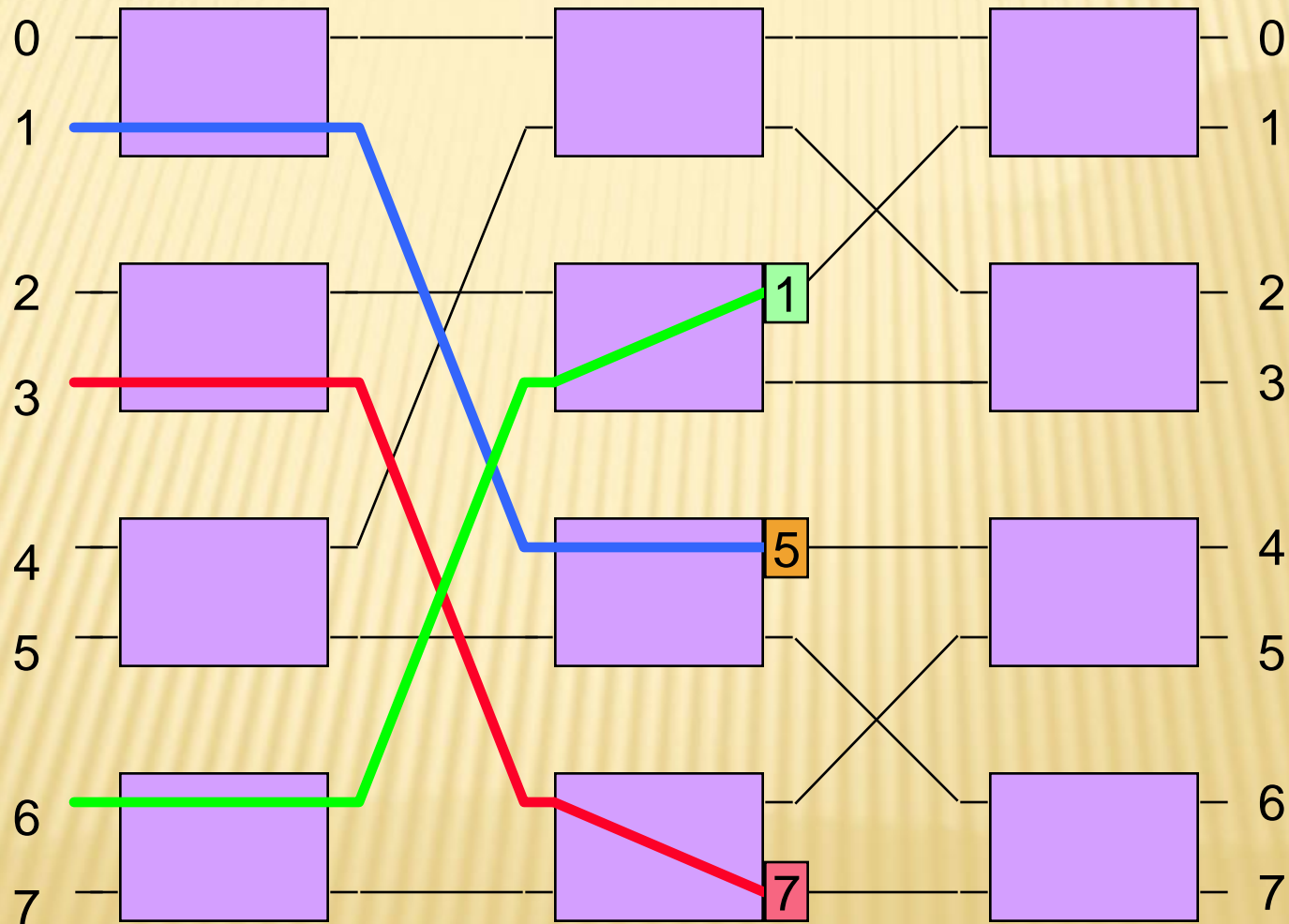
MULTIPLE CONCURRENT PATHS



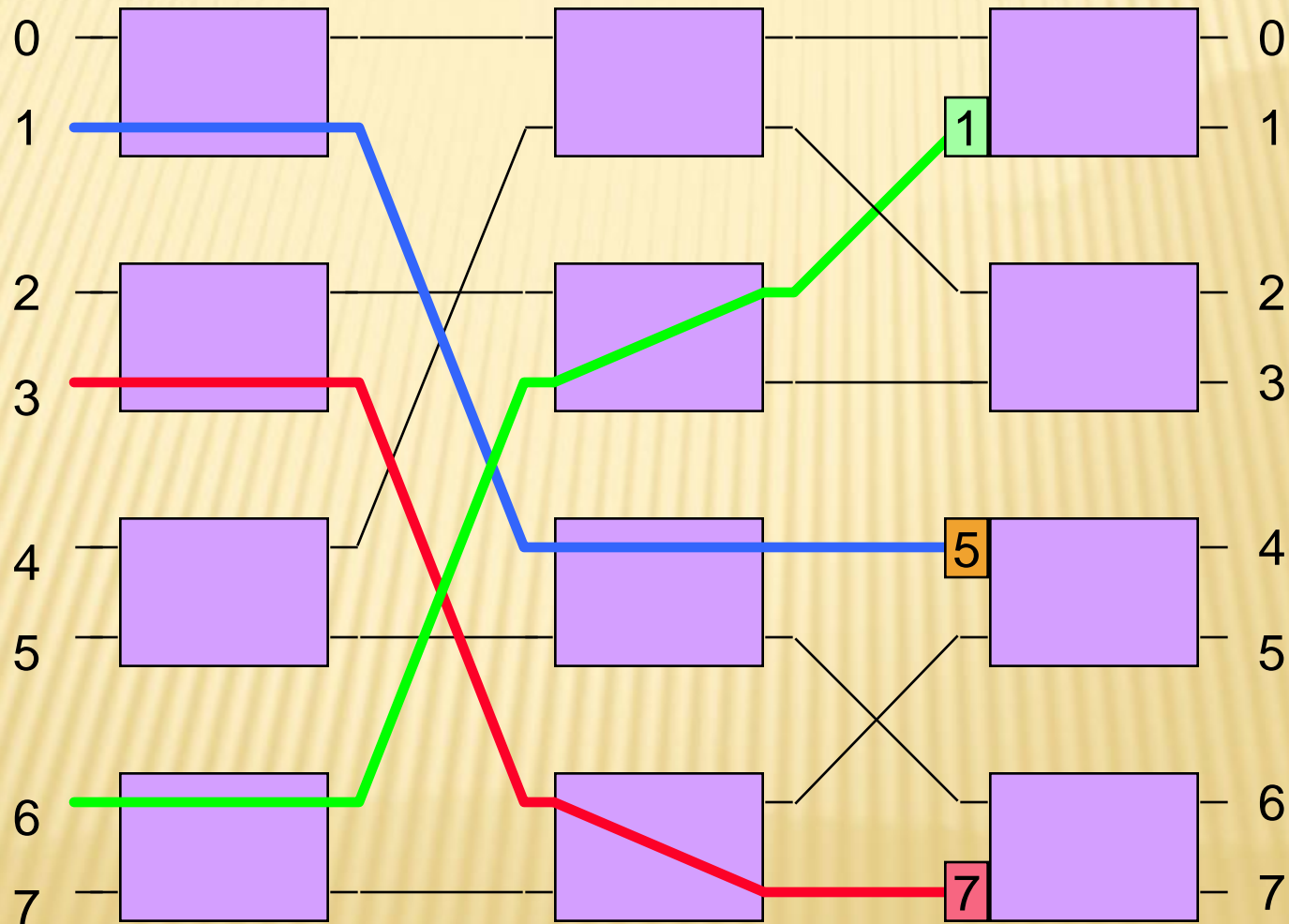
MULTIPLE CONCURRENT PATHS



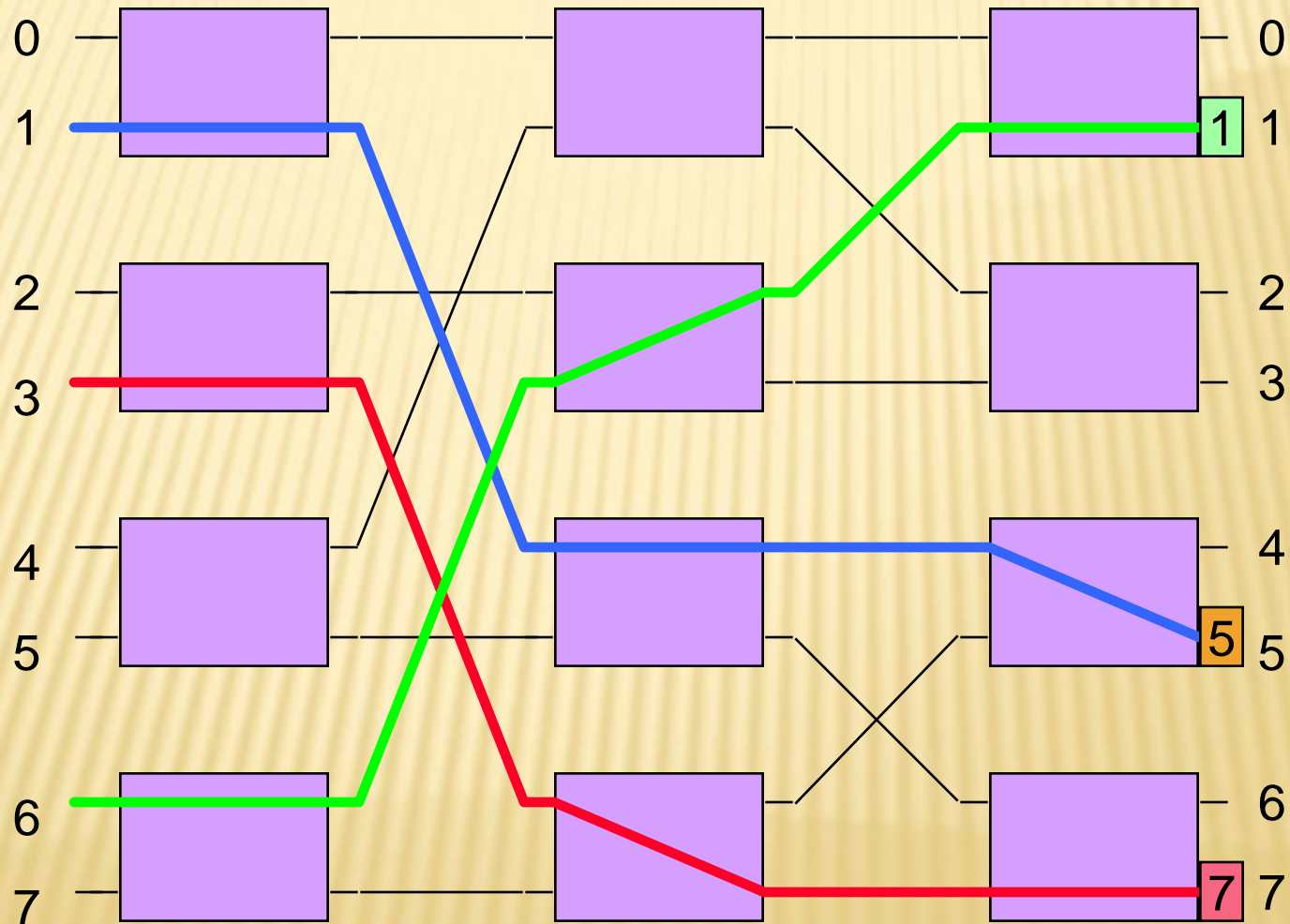
MULTIPLE CONCURRENT PATHS



MULTIPLE CONCURRENT PATHS



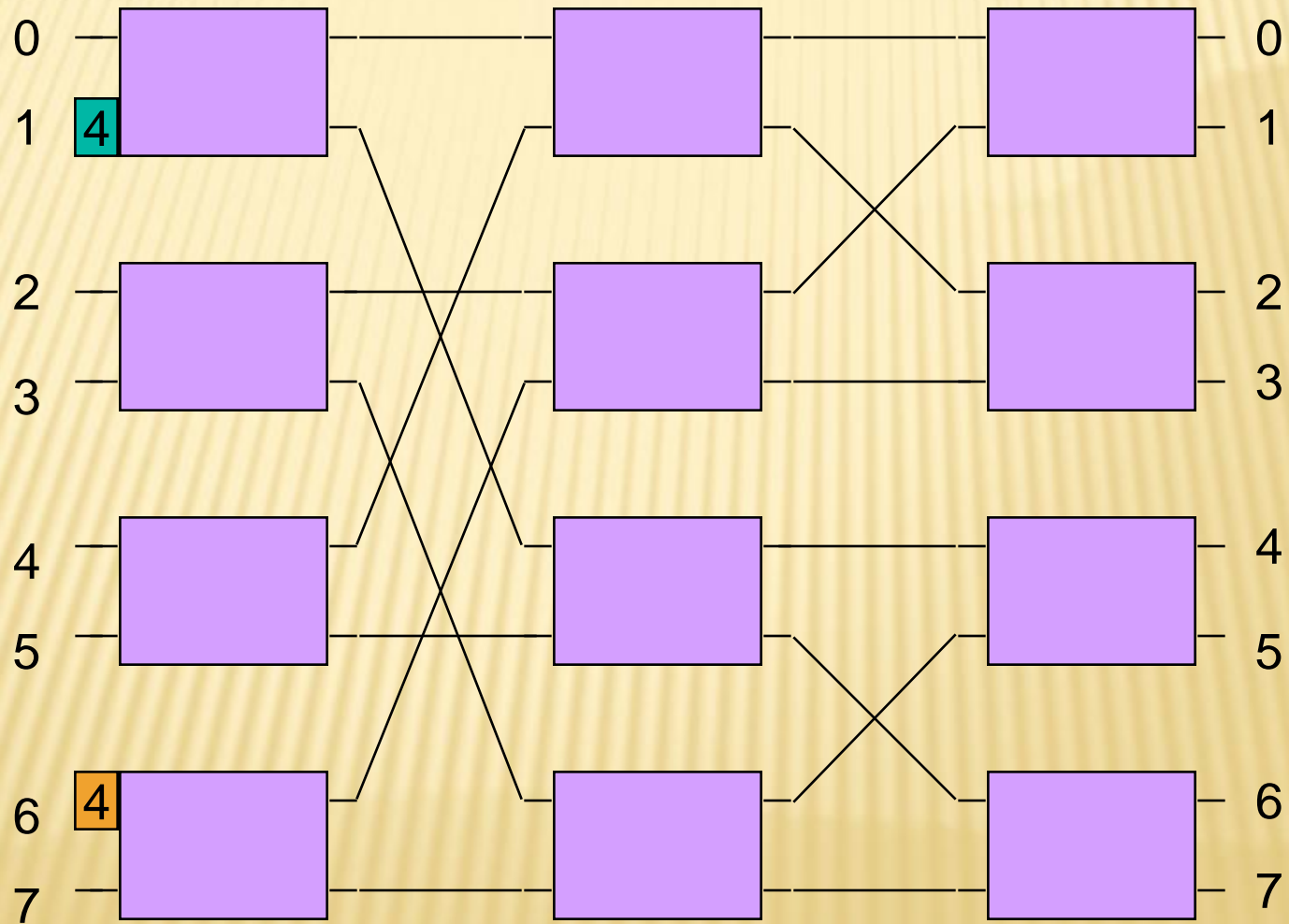
MULTIPLE CONCURRENT PATHS



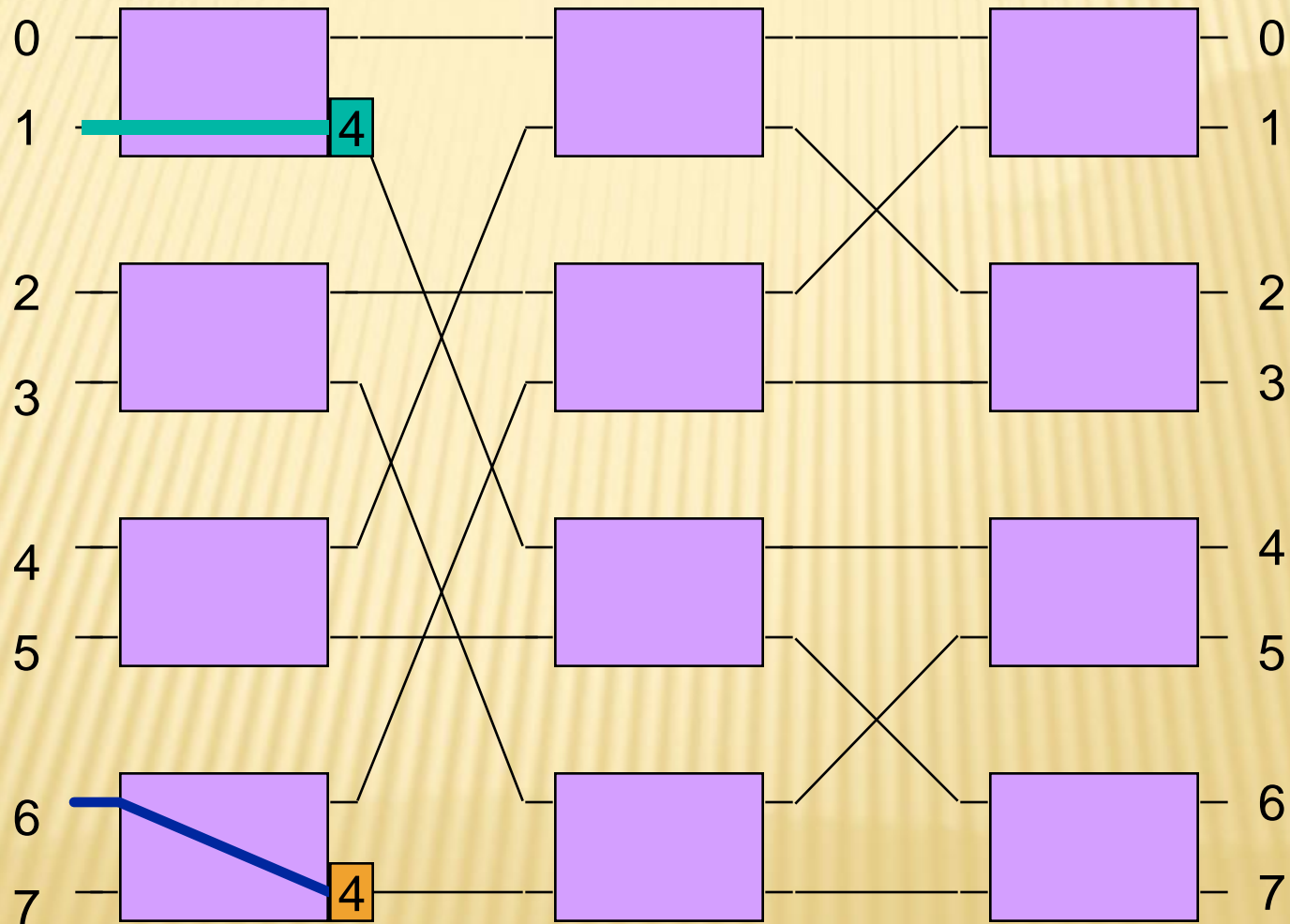
OUTPUT PORT CONTENTION

- Up to now, all examples have worked wonderfully because each incoming cell was destined to a different output port
- What happens if more than one cell destined to same output port?
- Answer: output port contention
- Result: cell loss in a bufferless network

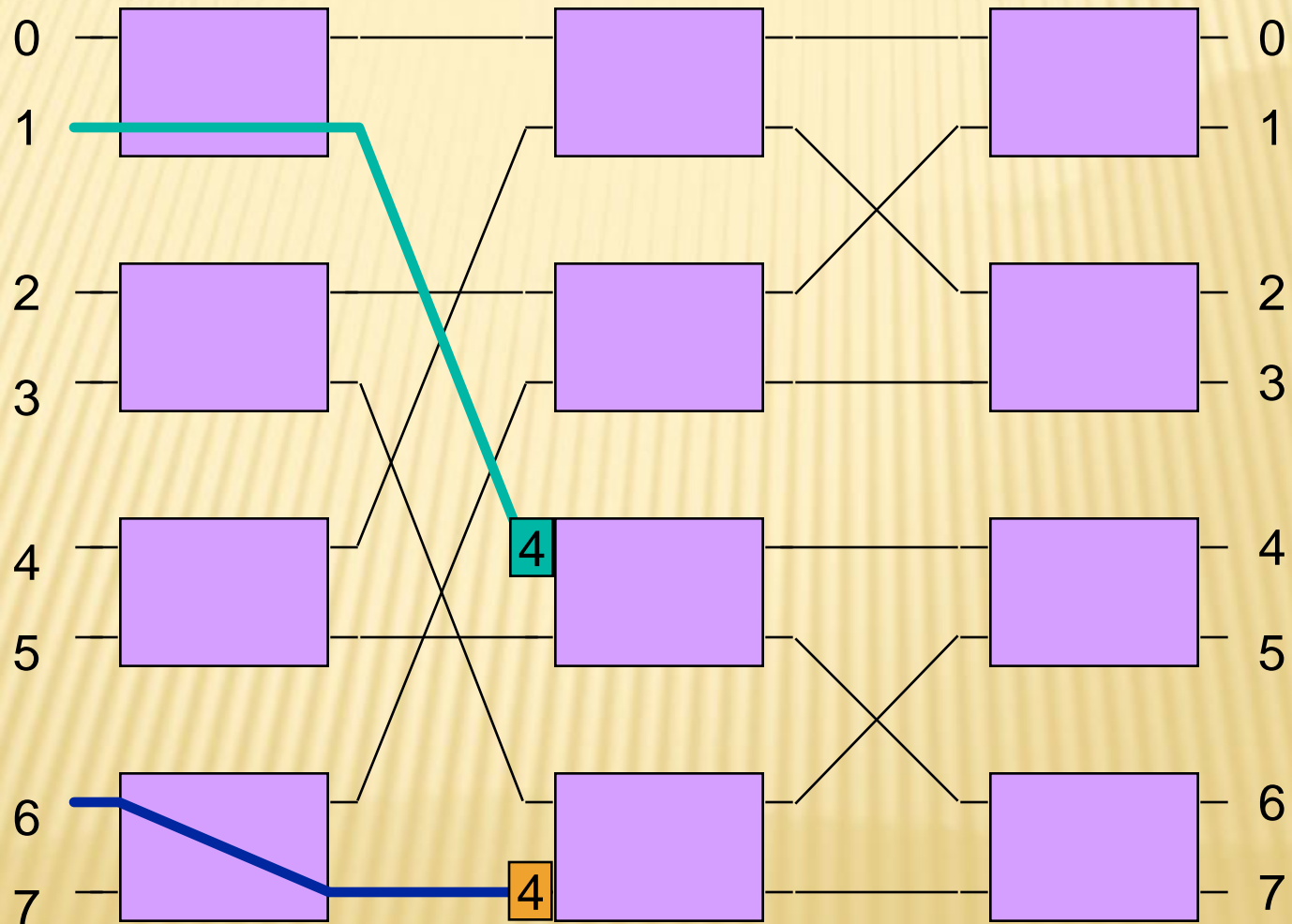
OUTPUT PORT CONTENTION



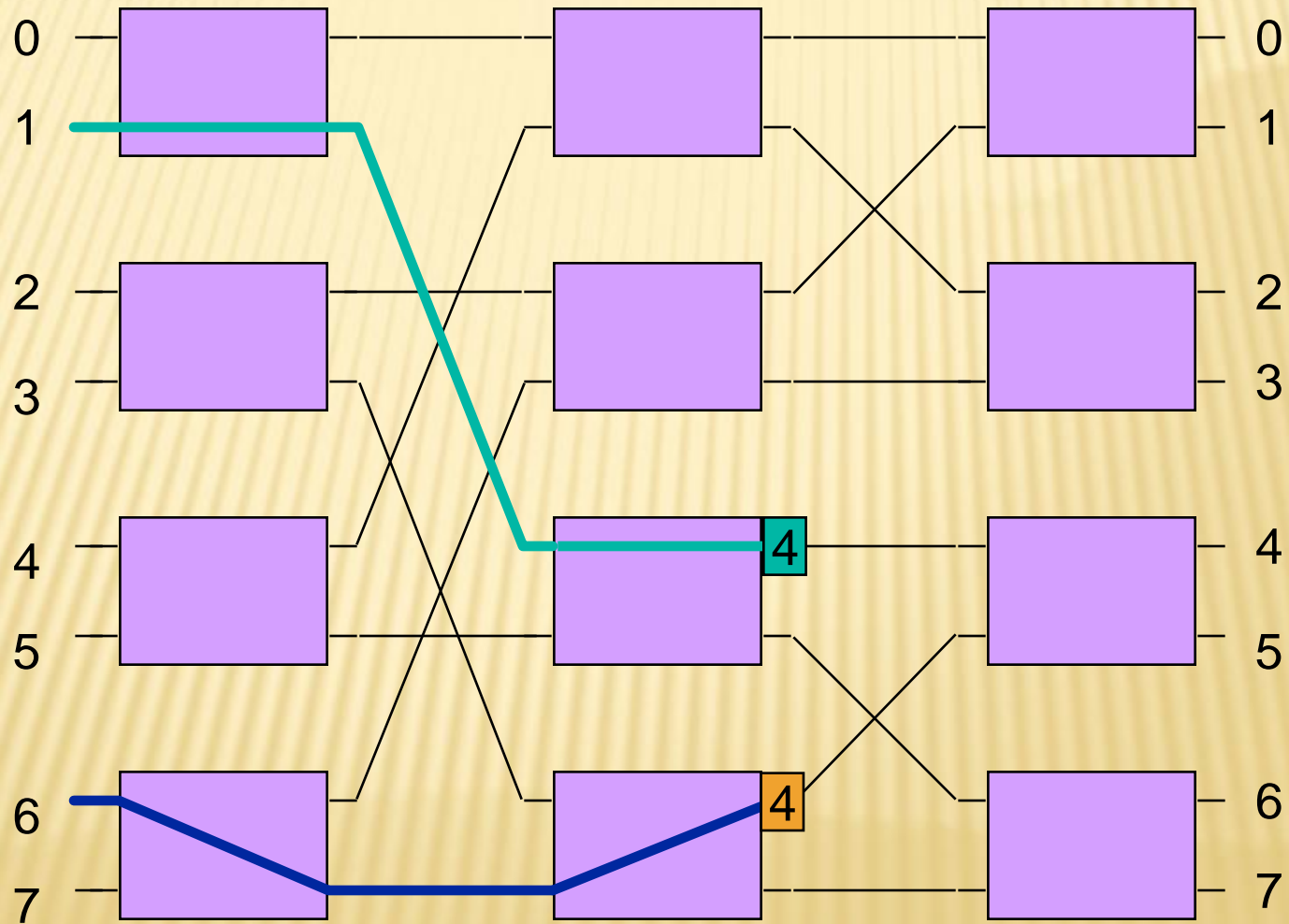
OUTPUT PORT CONTENTION



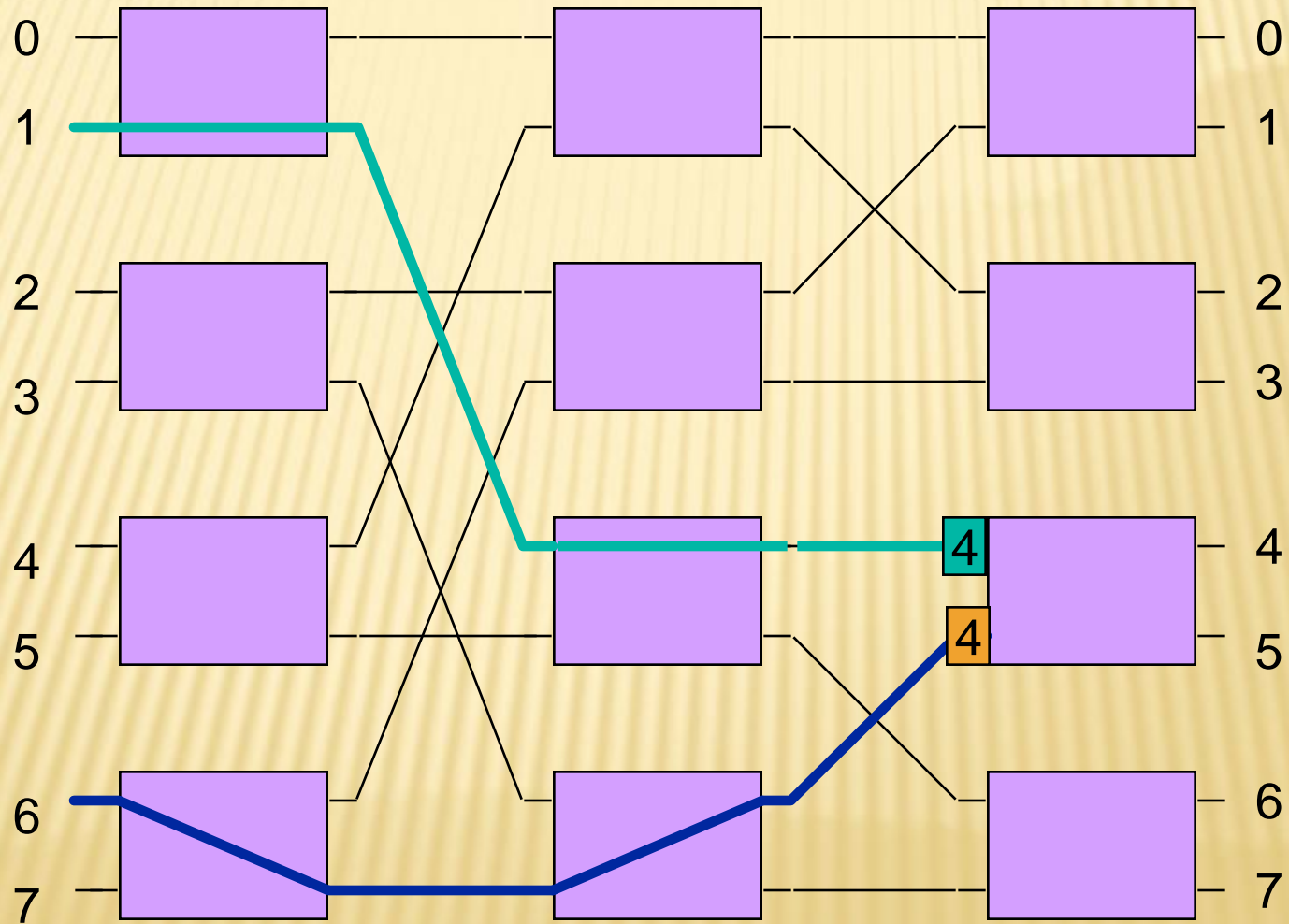
OUTPUT PORT CONTENTION



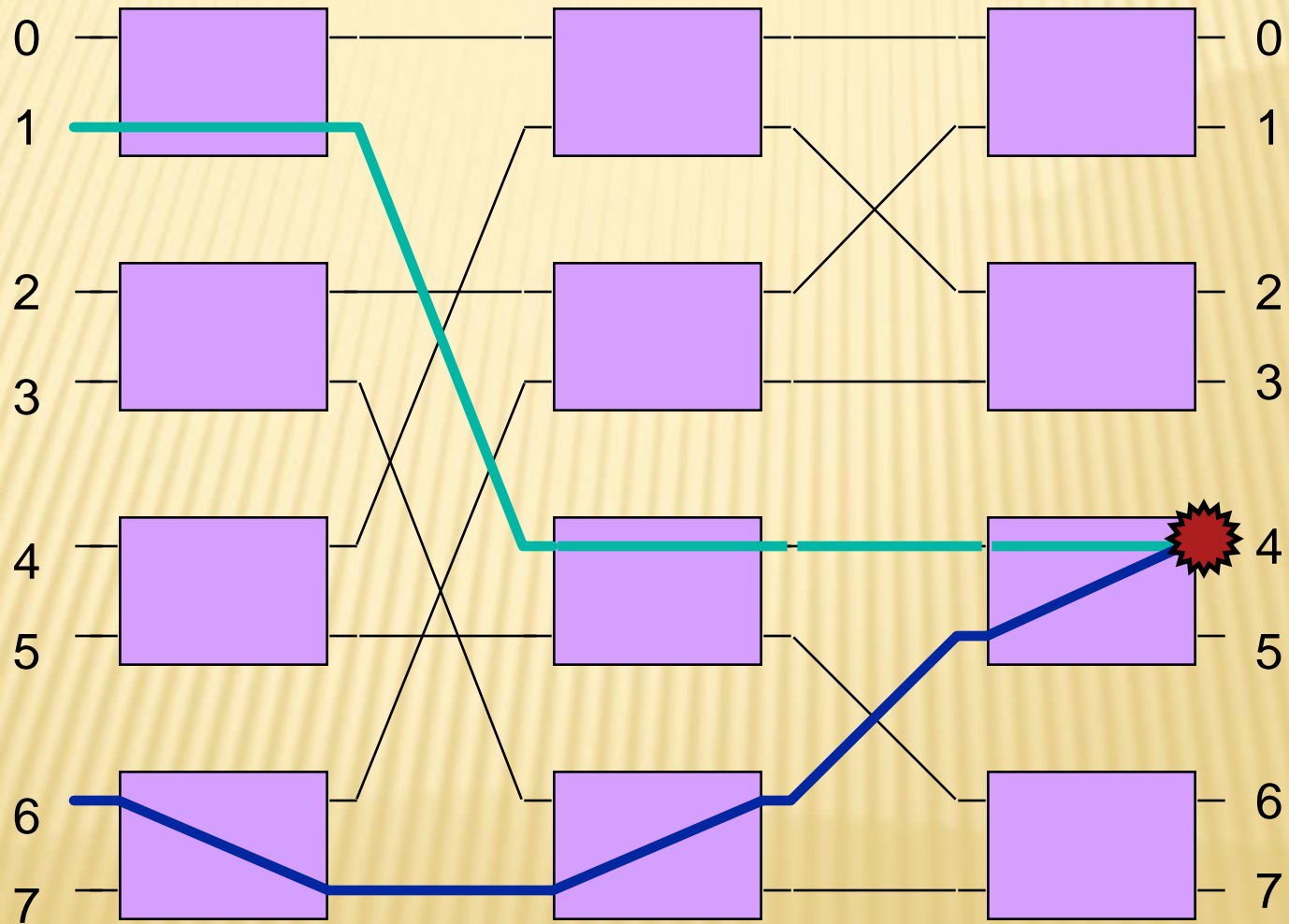
OUTPUT PORT CONTENTION



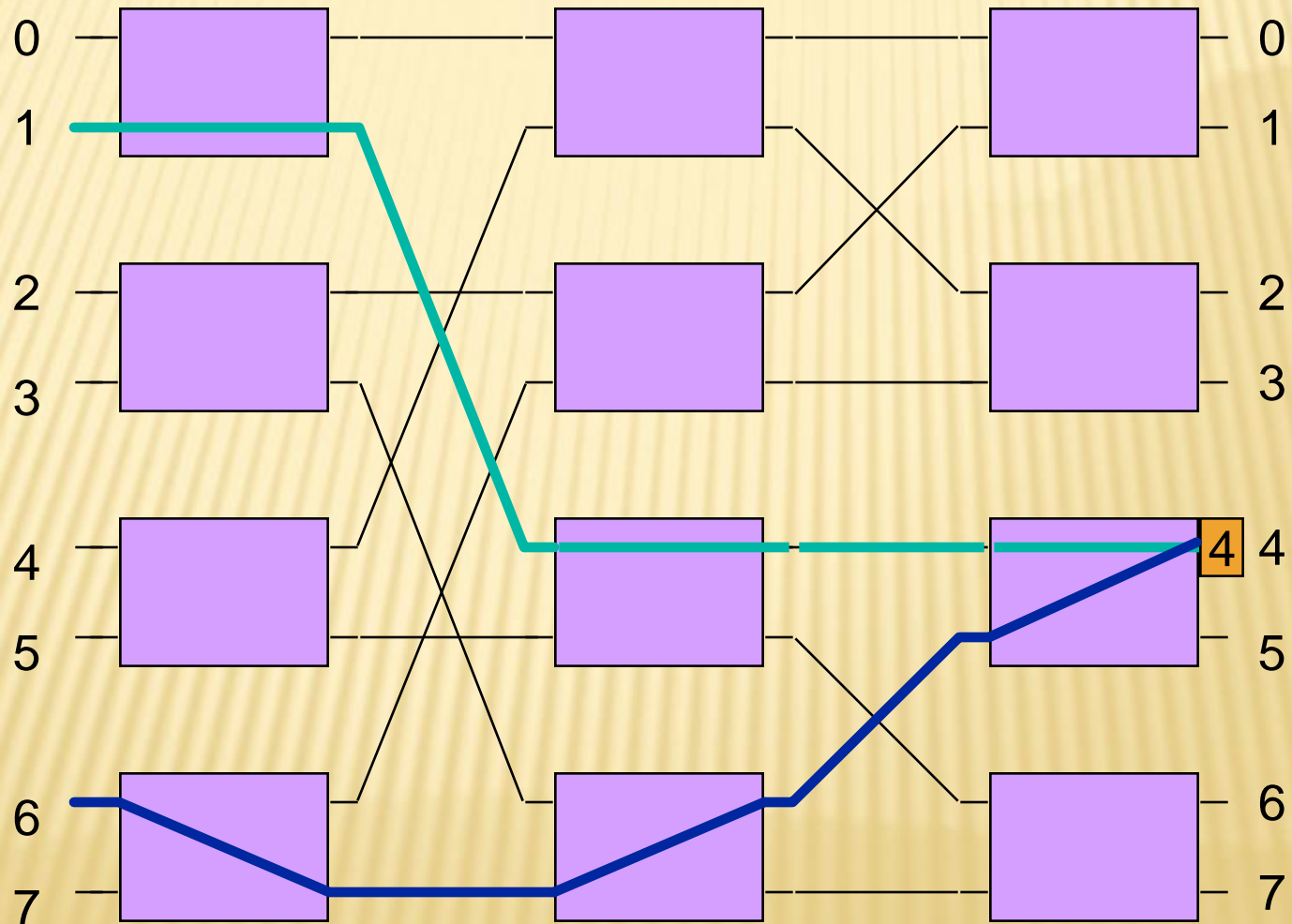
OUTPUT PORT CONTENTION



OUTPUT PORT CONTENTION



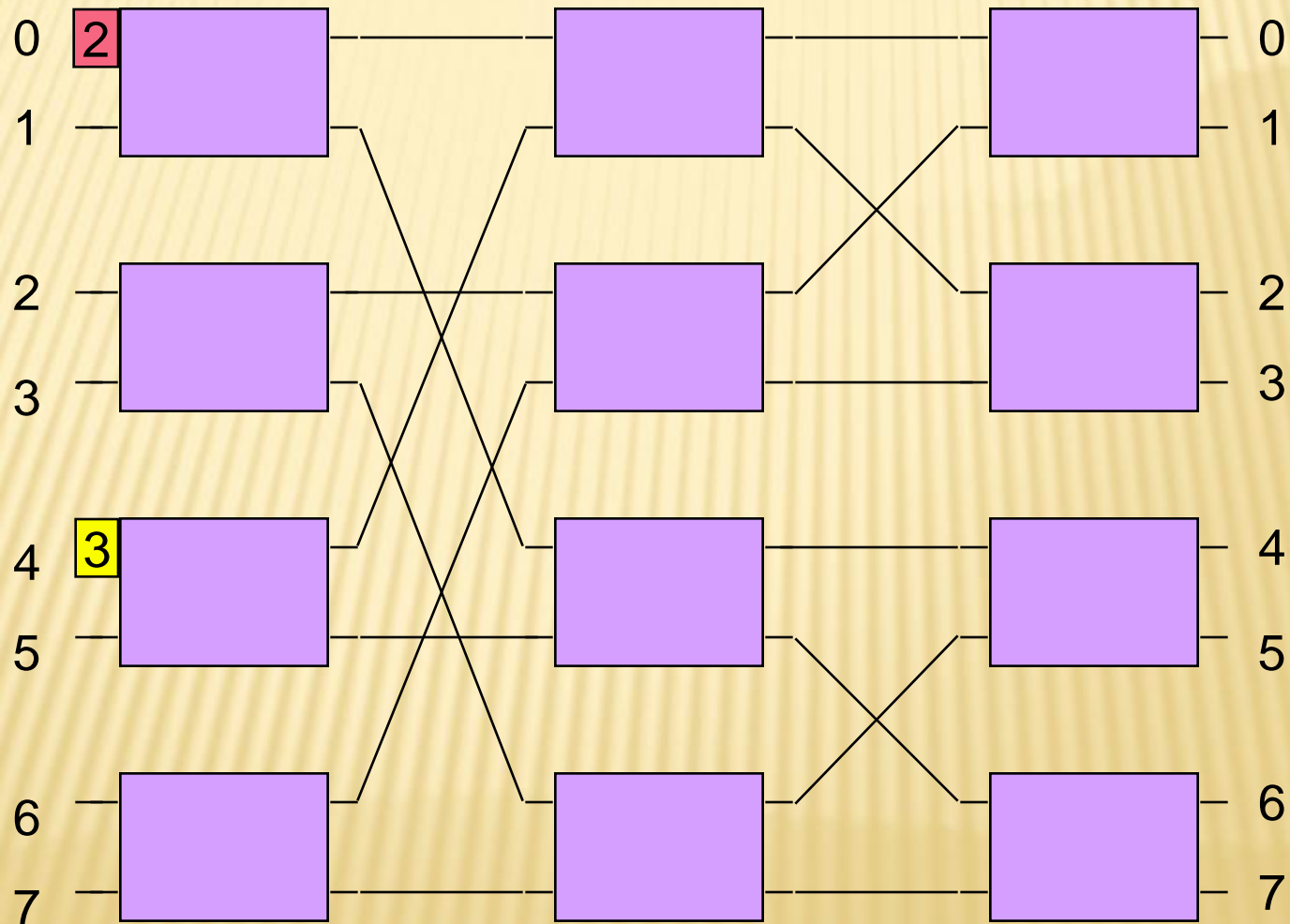
OUTPUT PORT CONTENTION



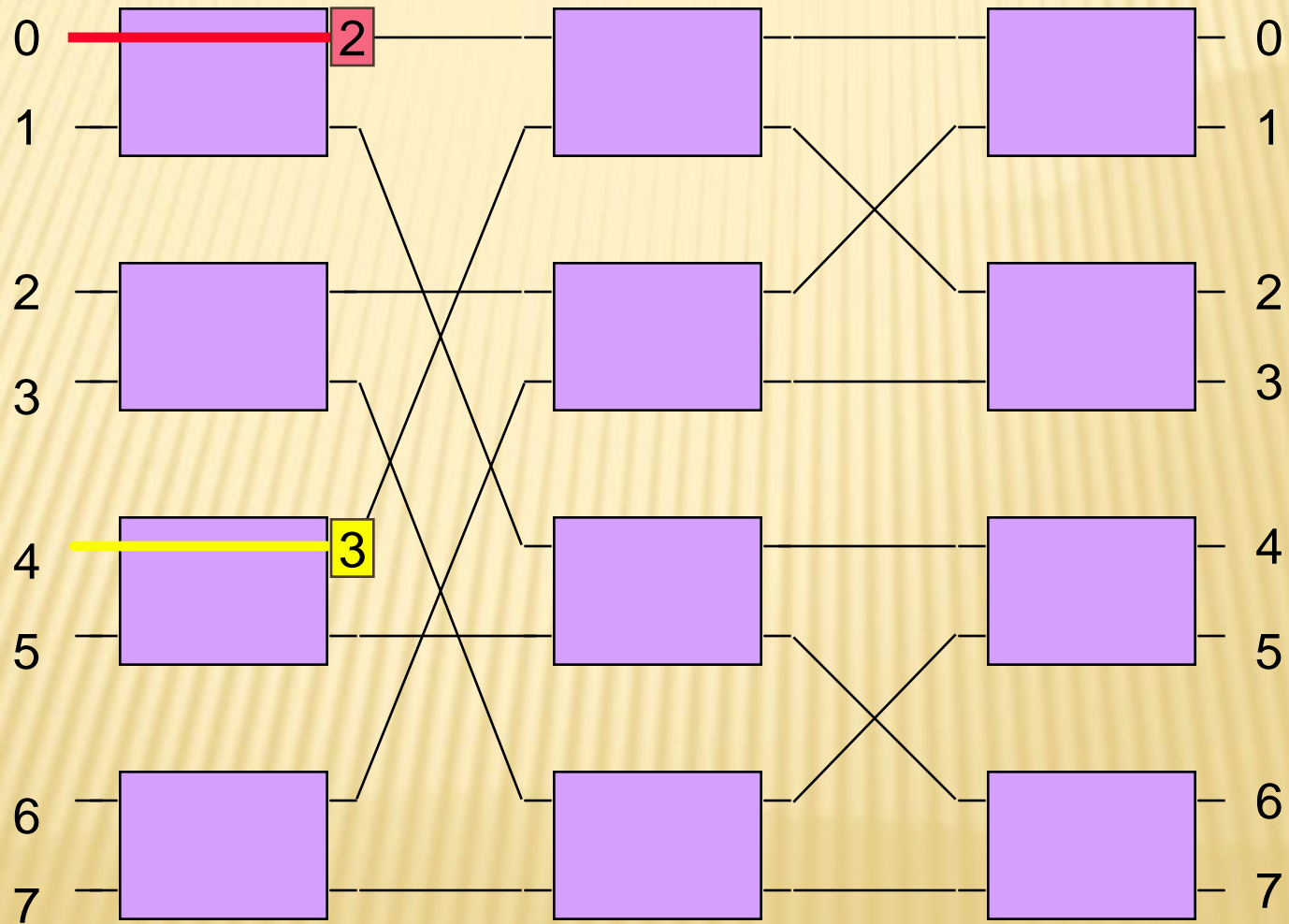
PATH CONTENTION

- ✘ It is also possible for two incoming cells that are destined to different output ports to require the same internal link in the switch
- ✘ Called path contention or internal blocking
- ✘ Again, the result in a bufferless switch fabric is cell loss (one cell wins, one loses)
- ✘ Path contention and output port contention can seriously degrade the achievable throughput of the switch

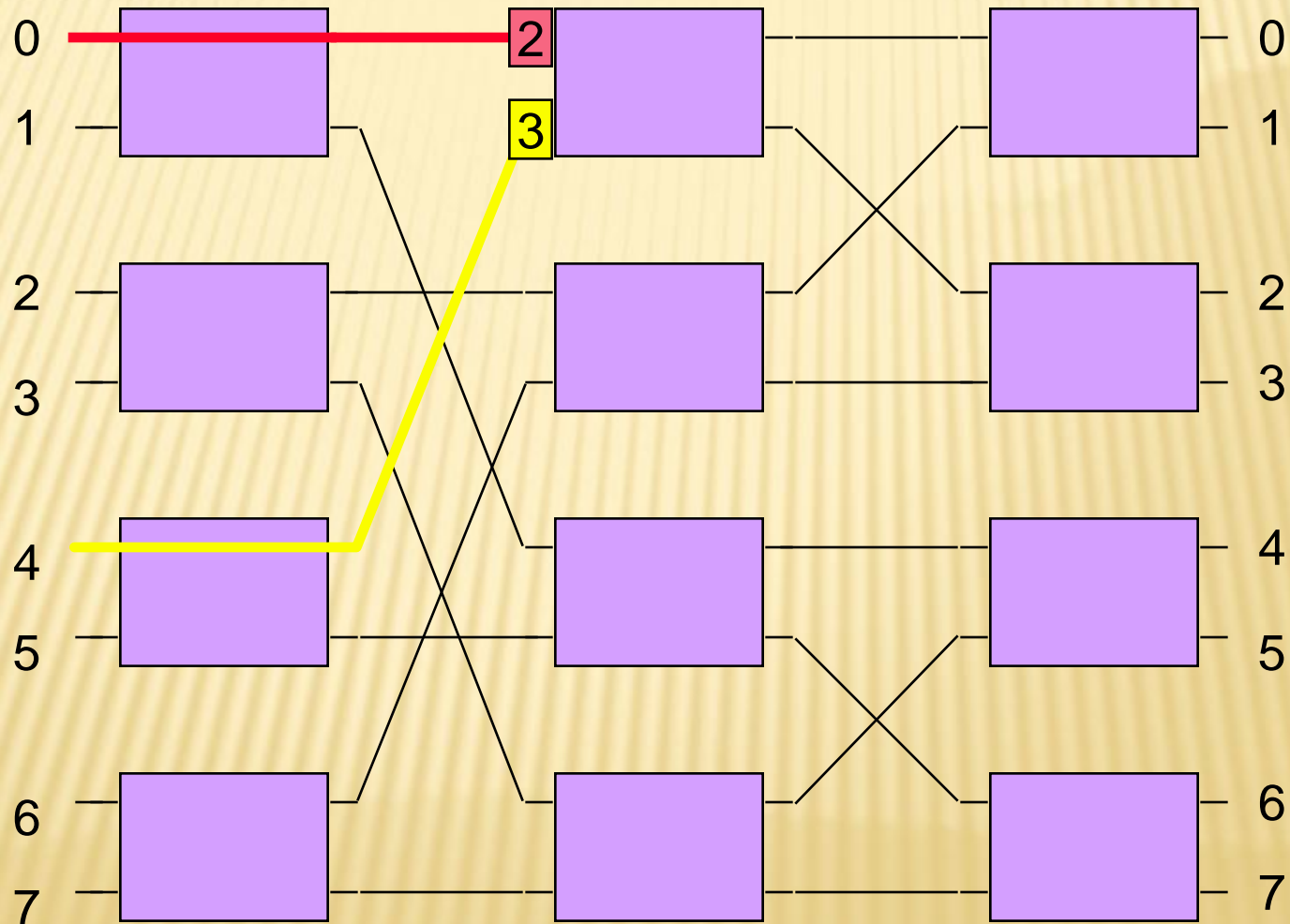
PATH CONTENTION



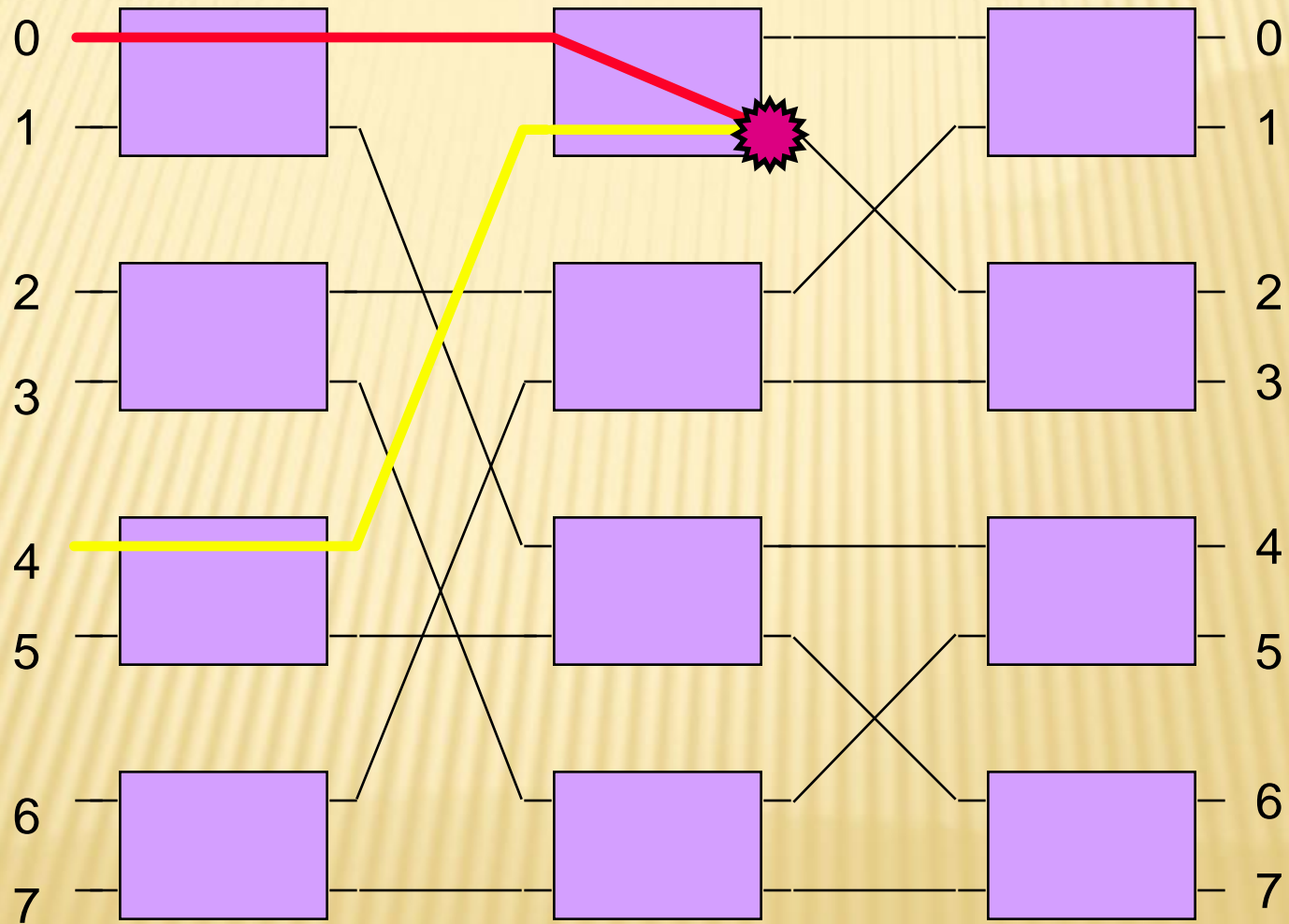
PATH CONTENTION



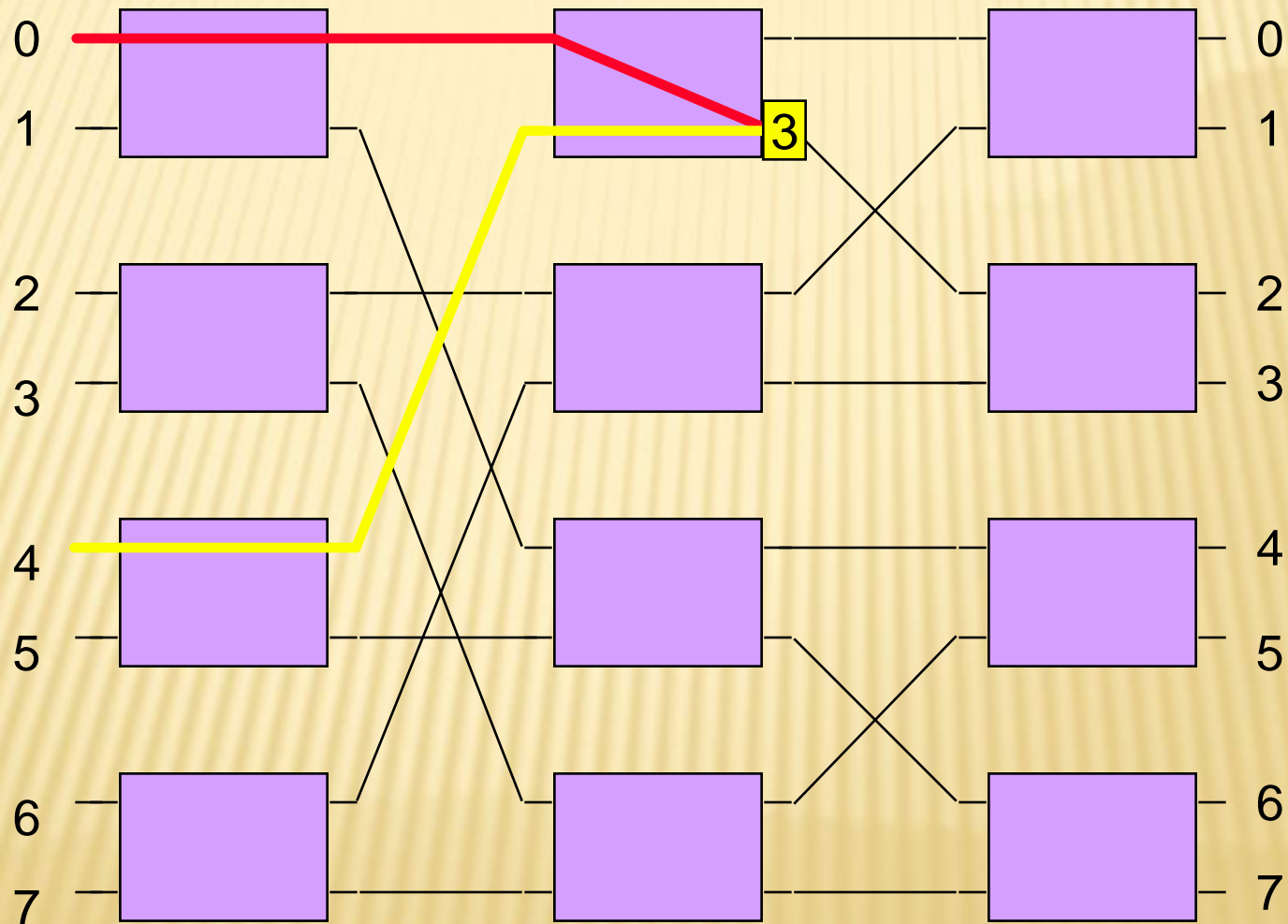
PATH CONTENTION



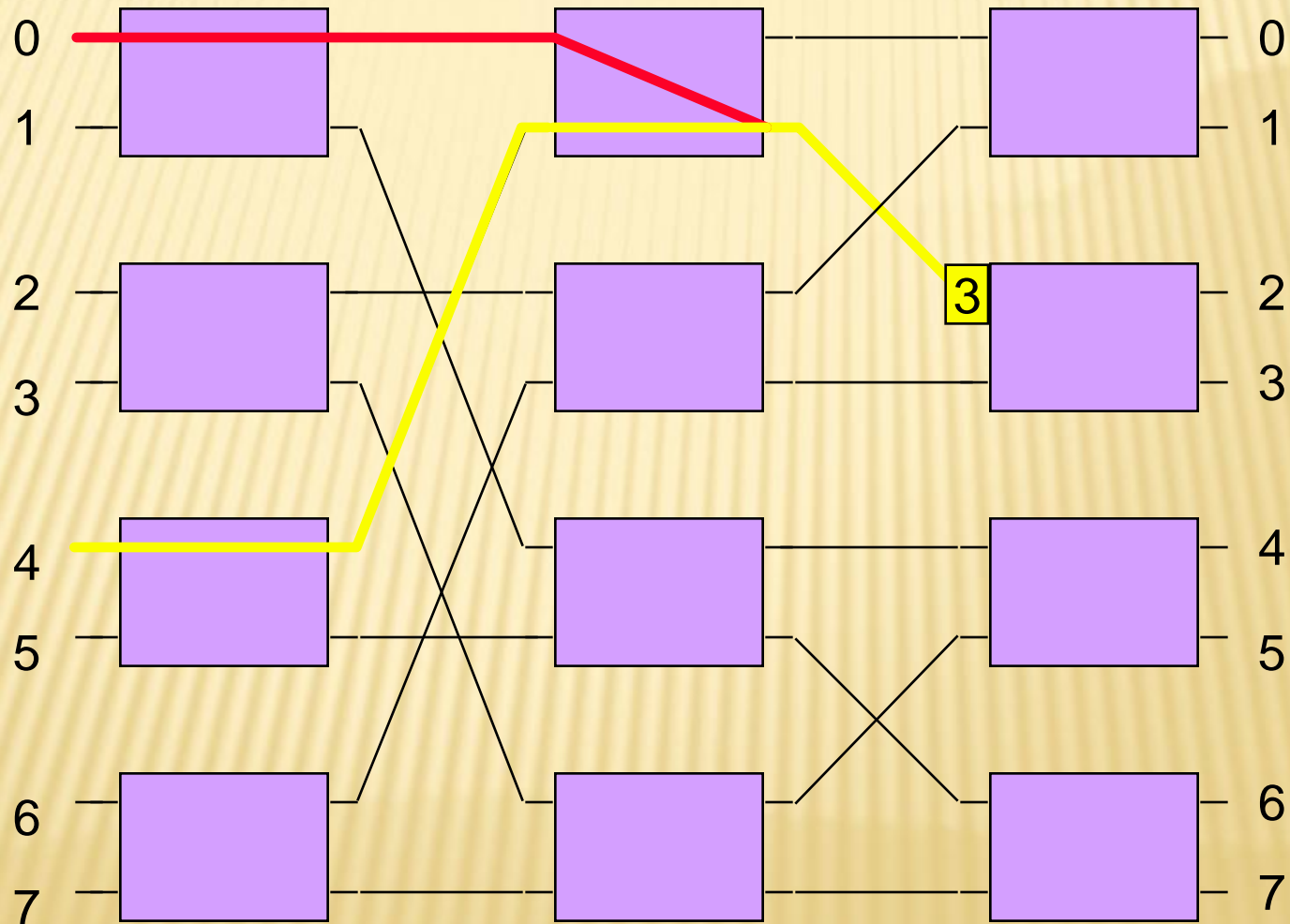
PATH CONTENTION



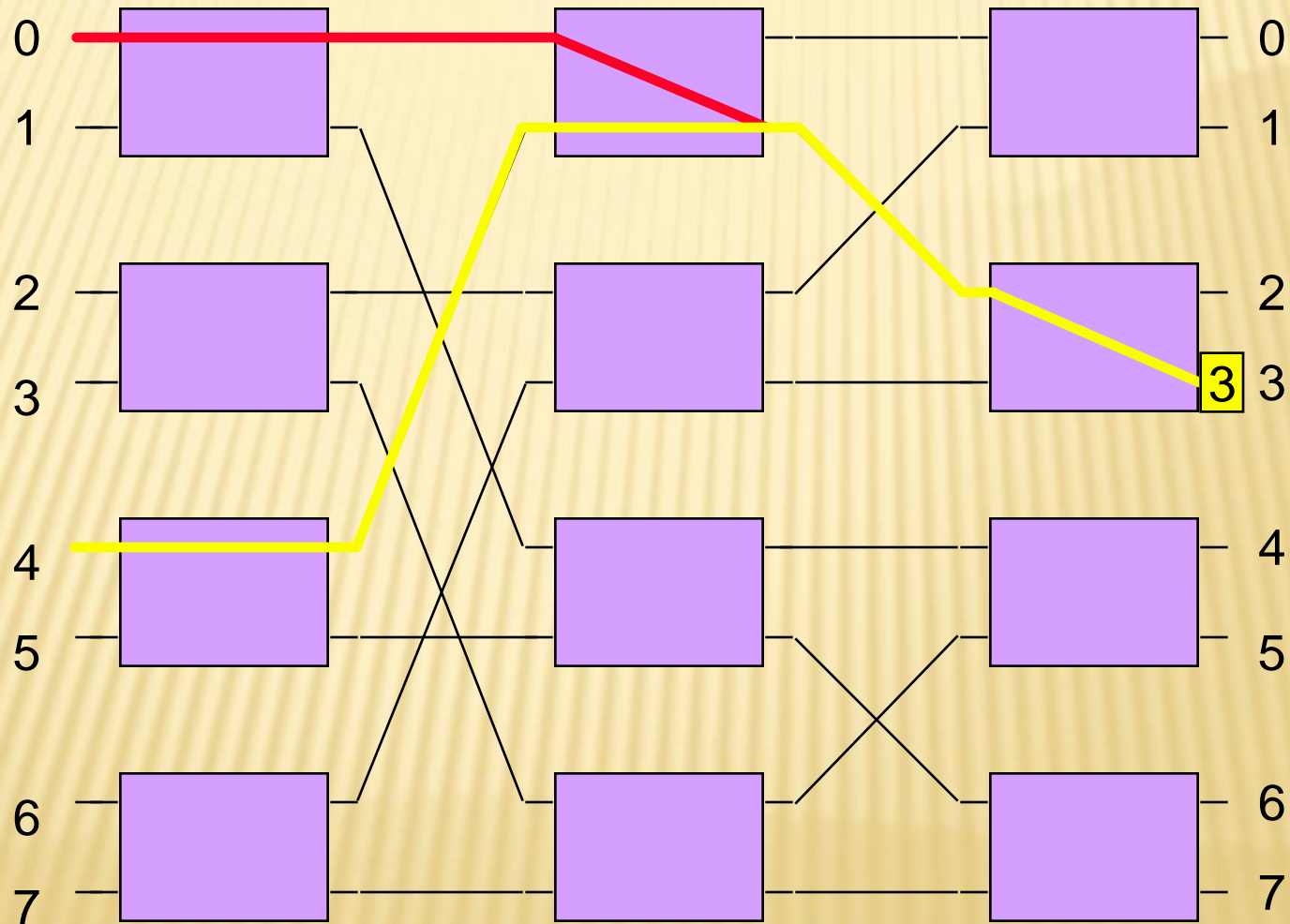
PATH CONTENTION



PATH CONTENTION

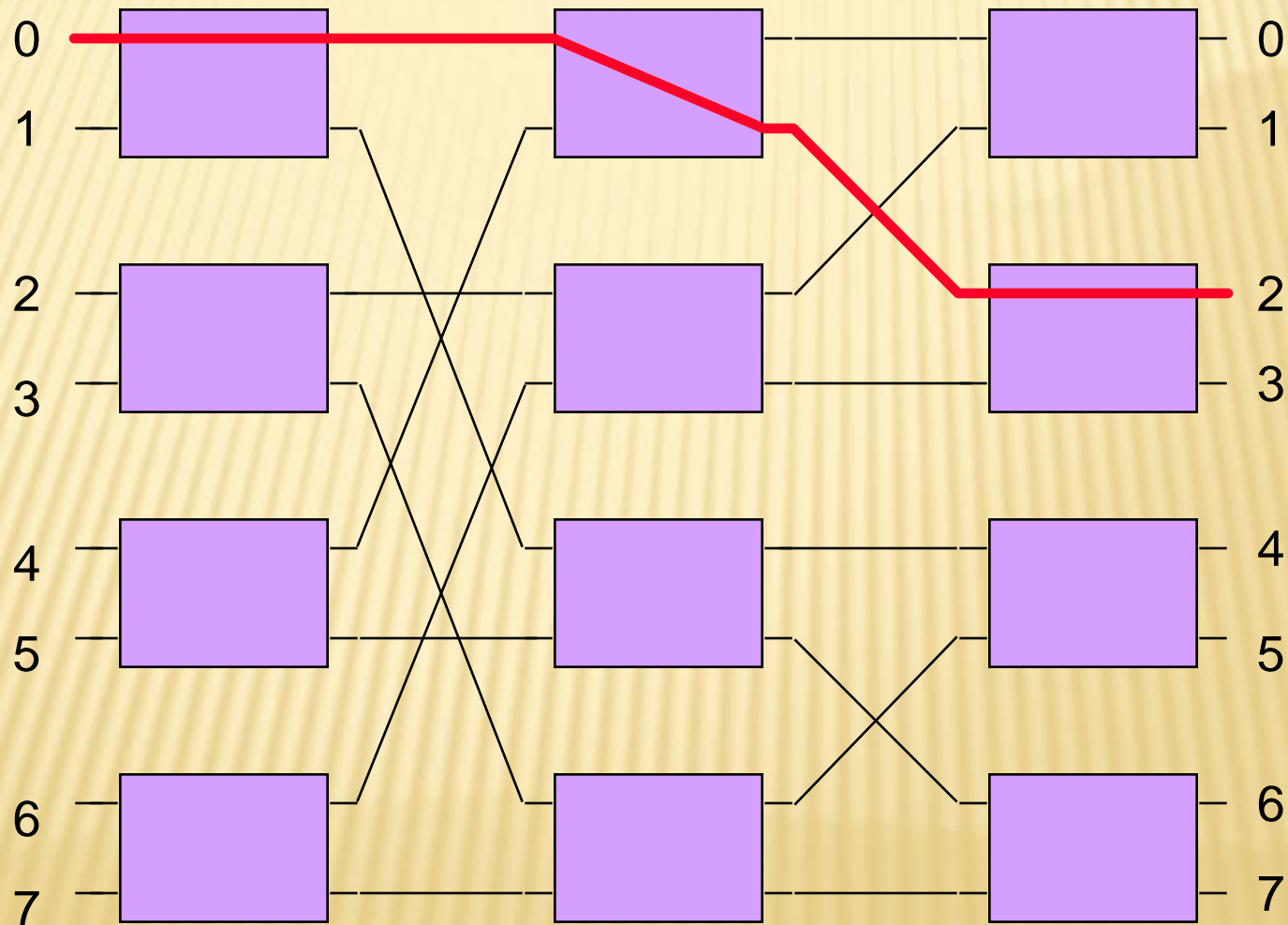


PATH CONTENTION



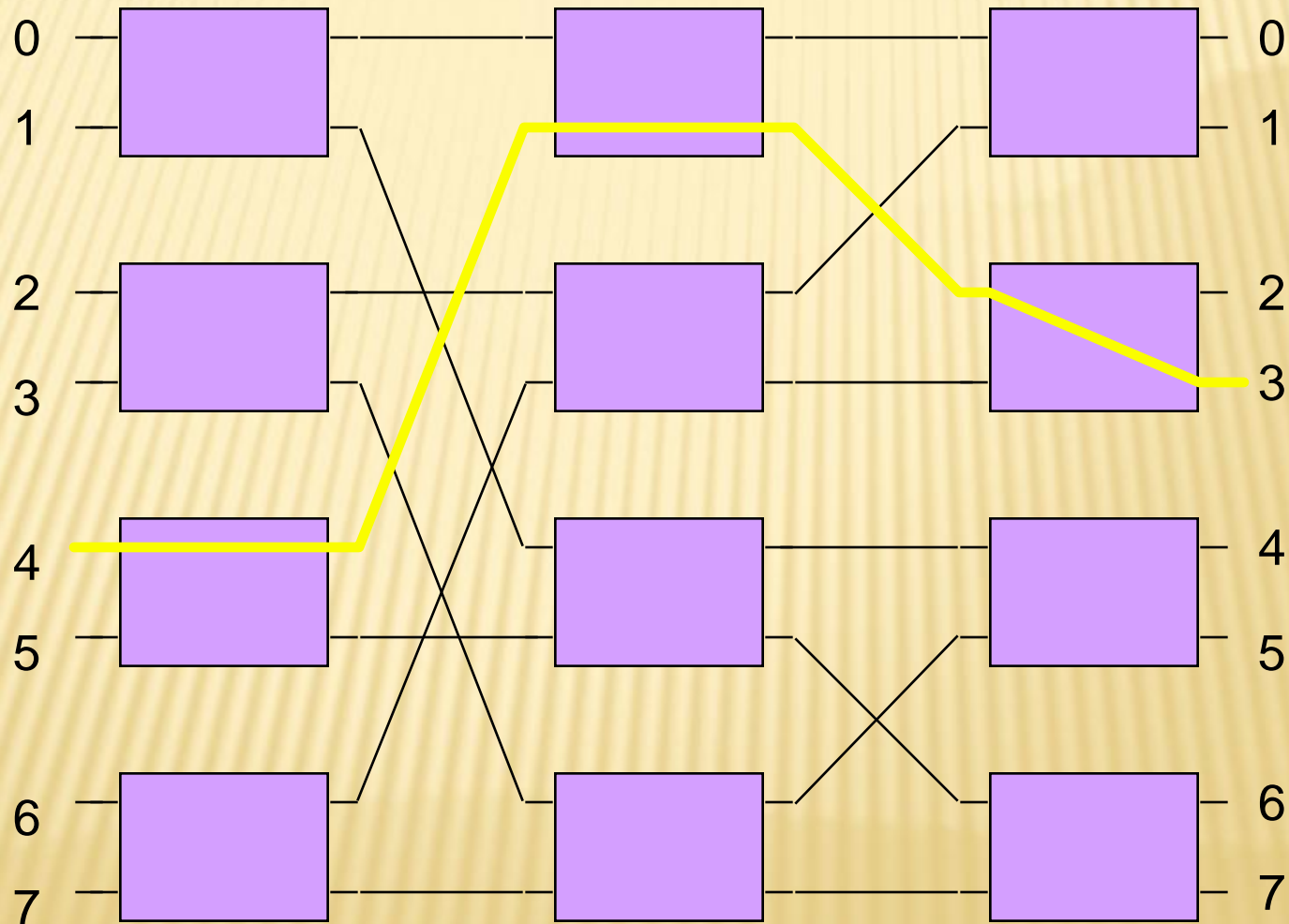
8 X 8 DELTA NETWORK

Cell on input port 0 destined for output port 2



8 x 8 DELTA NETWORK

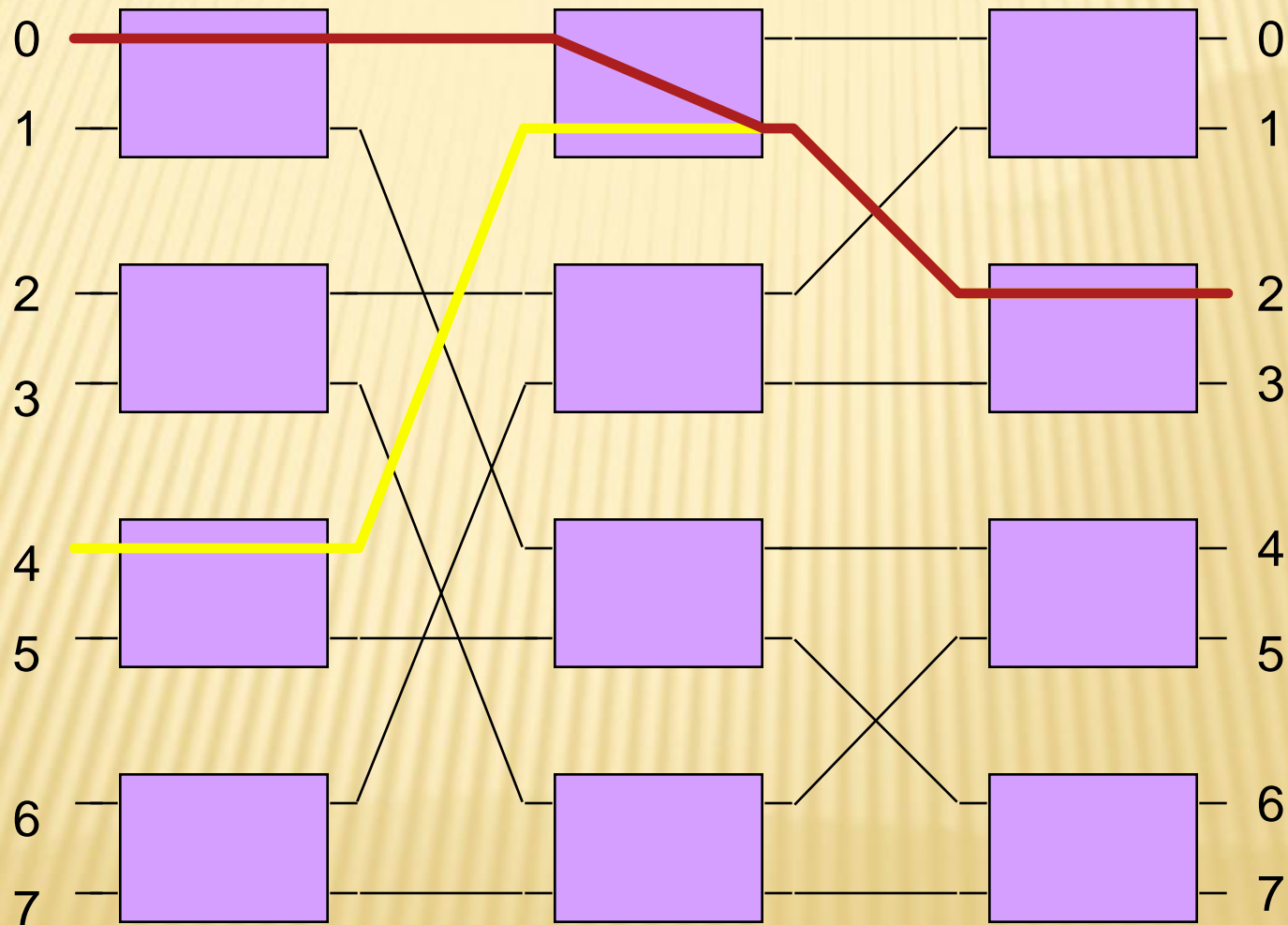
Cell on input port 4 destined for output port 3



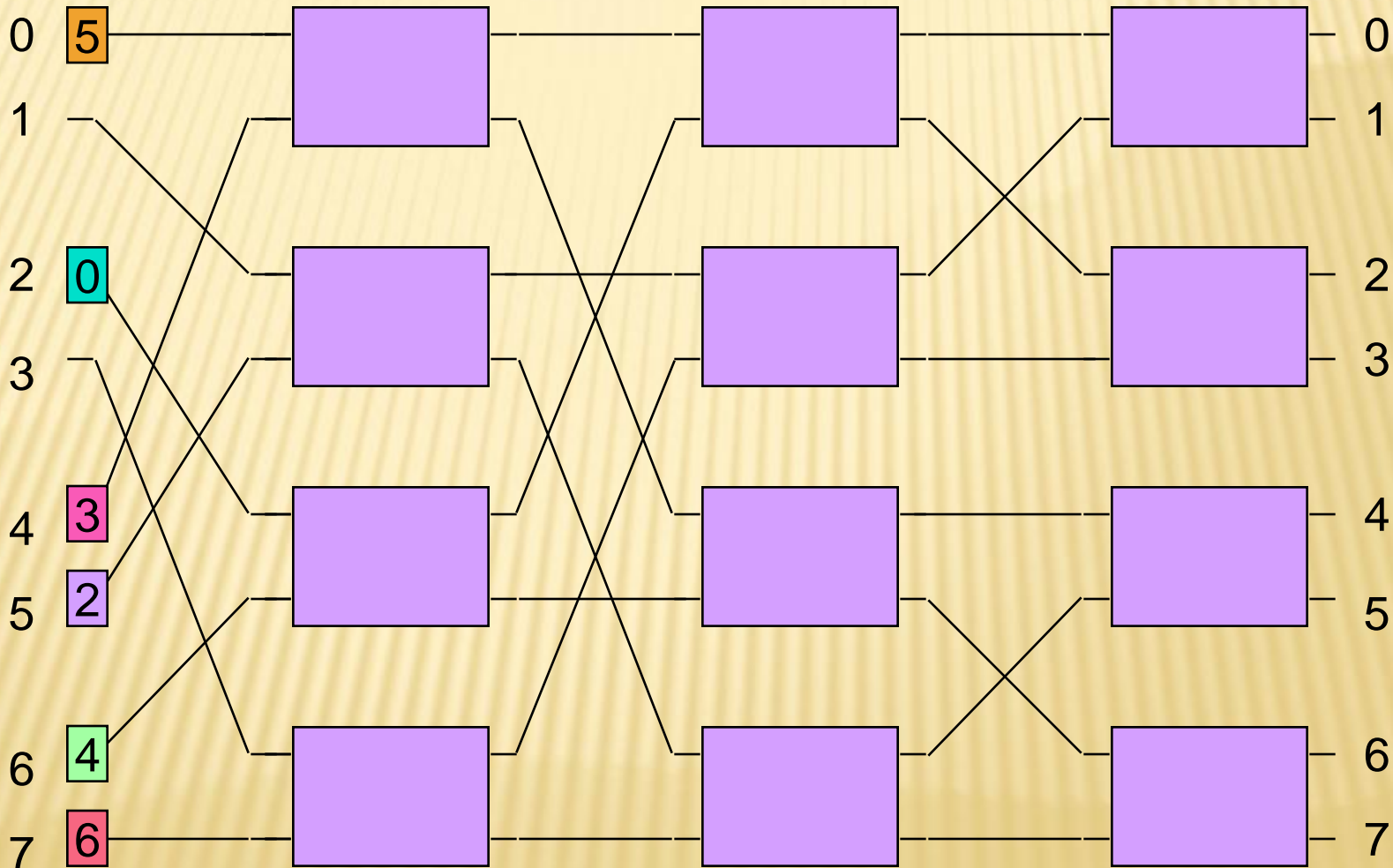
INTERNAL BLOCKING

Cell on input port 0 destined for output port 2

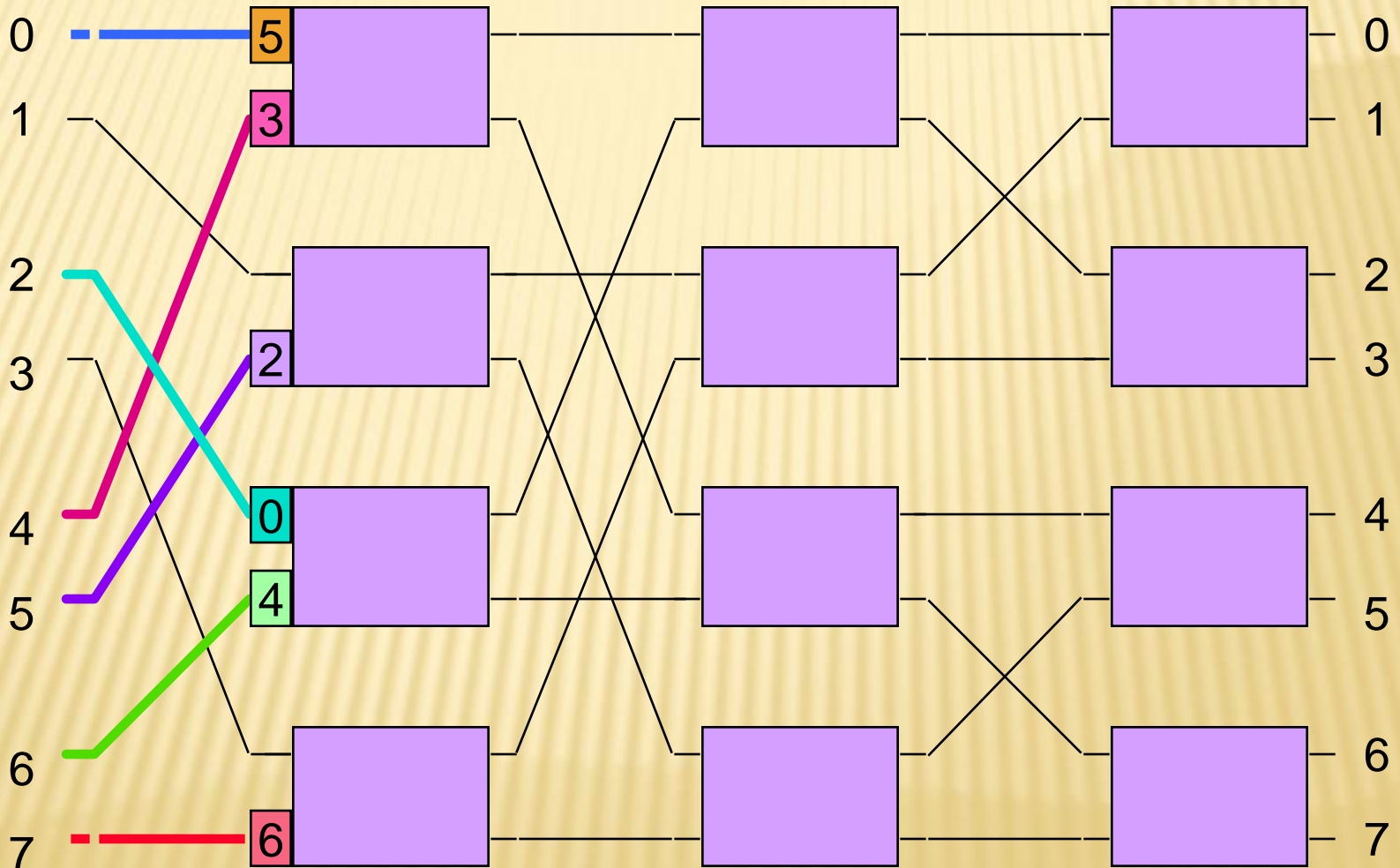
Cell on input port 4 destined for output port 3



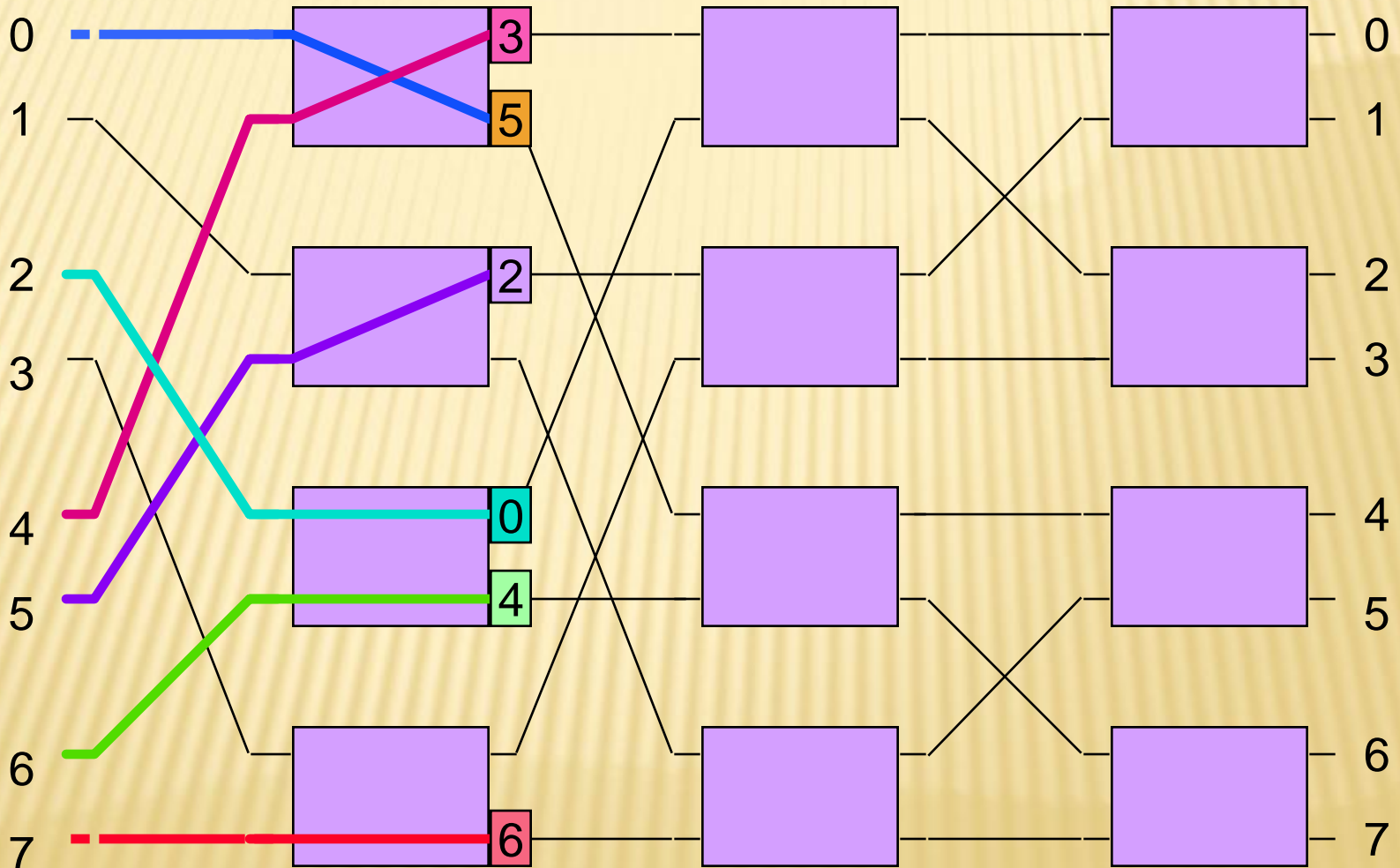
PERFORMANCE DEGRADATION



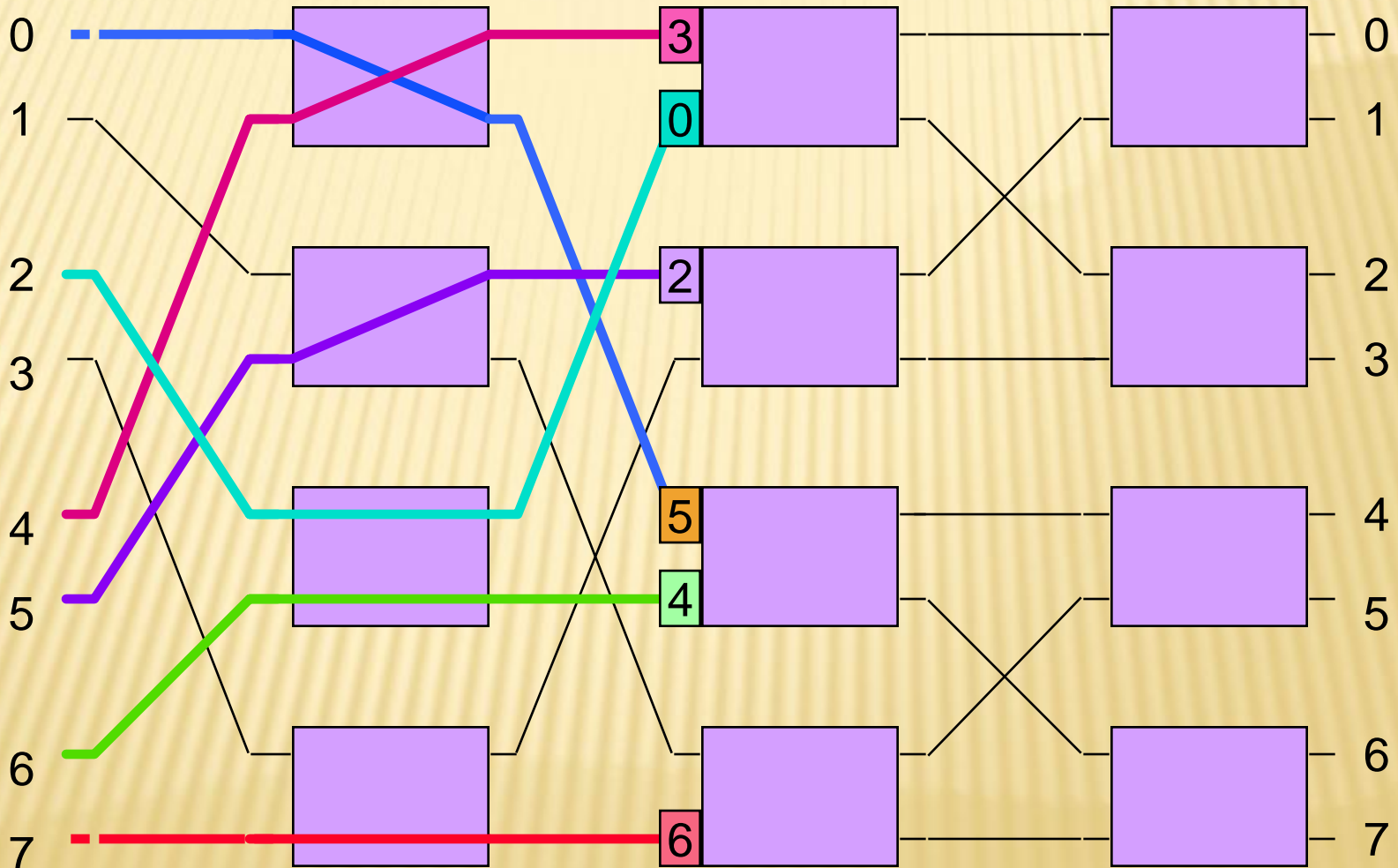
PERFORMANCE DEGRADATION



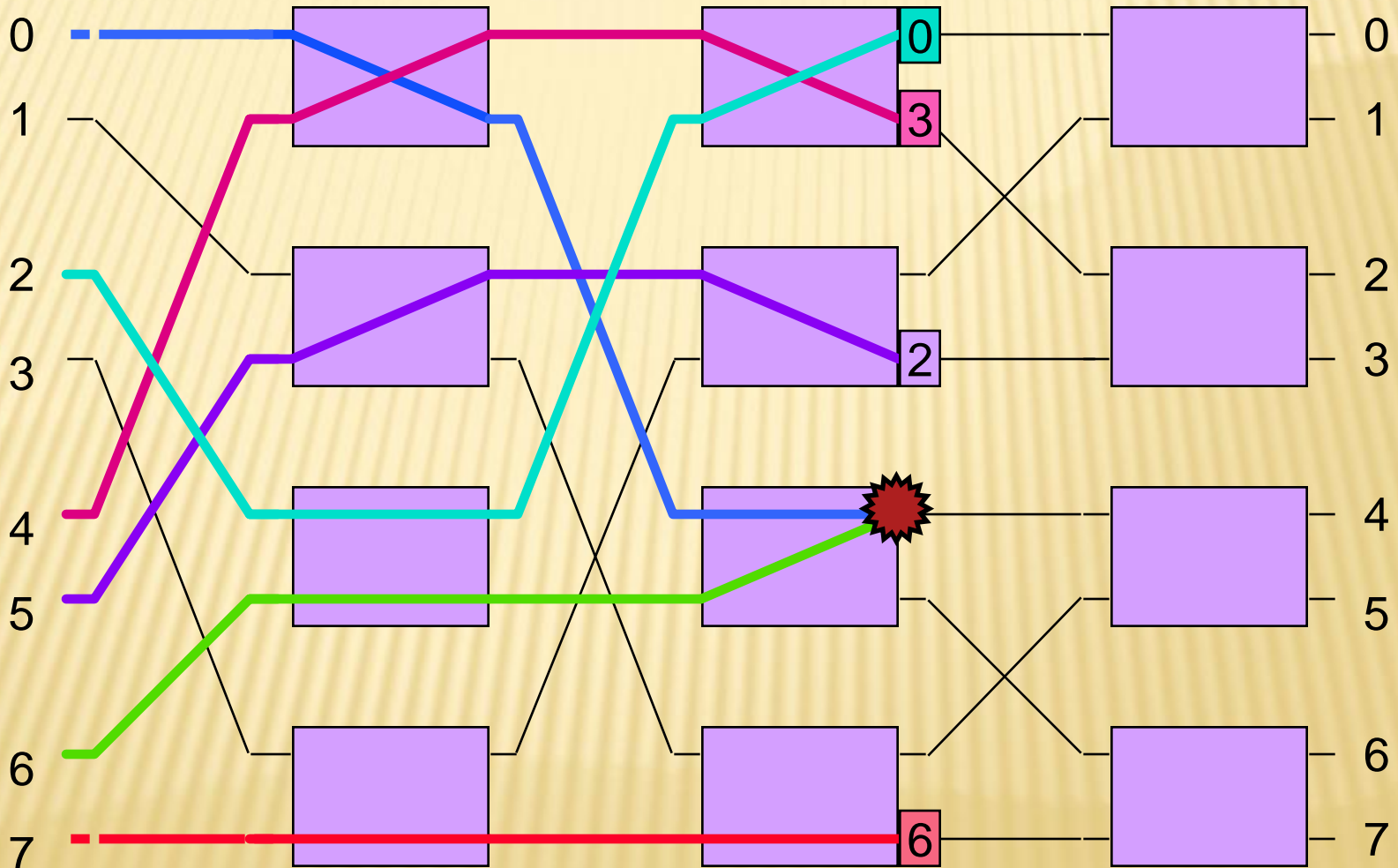
PERFORMANCE DEGRADATION



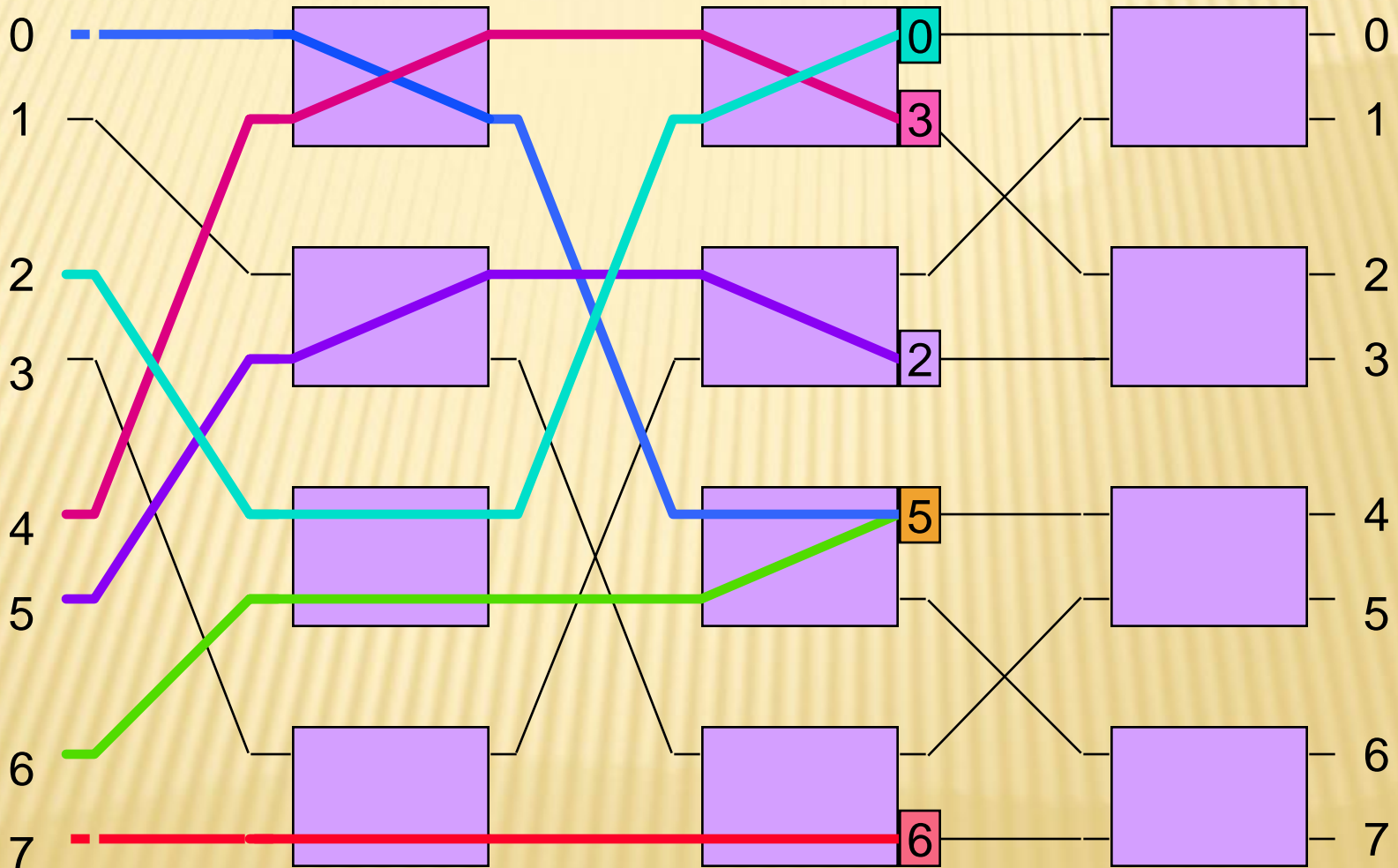
PERFORMANCE DEGRADATION



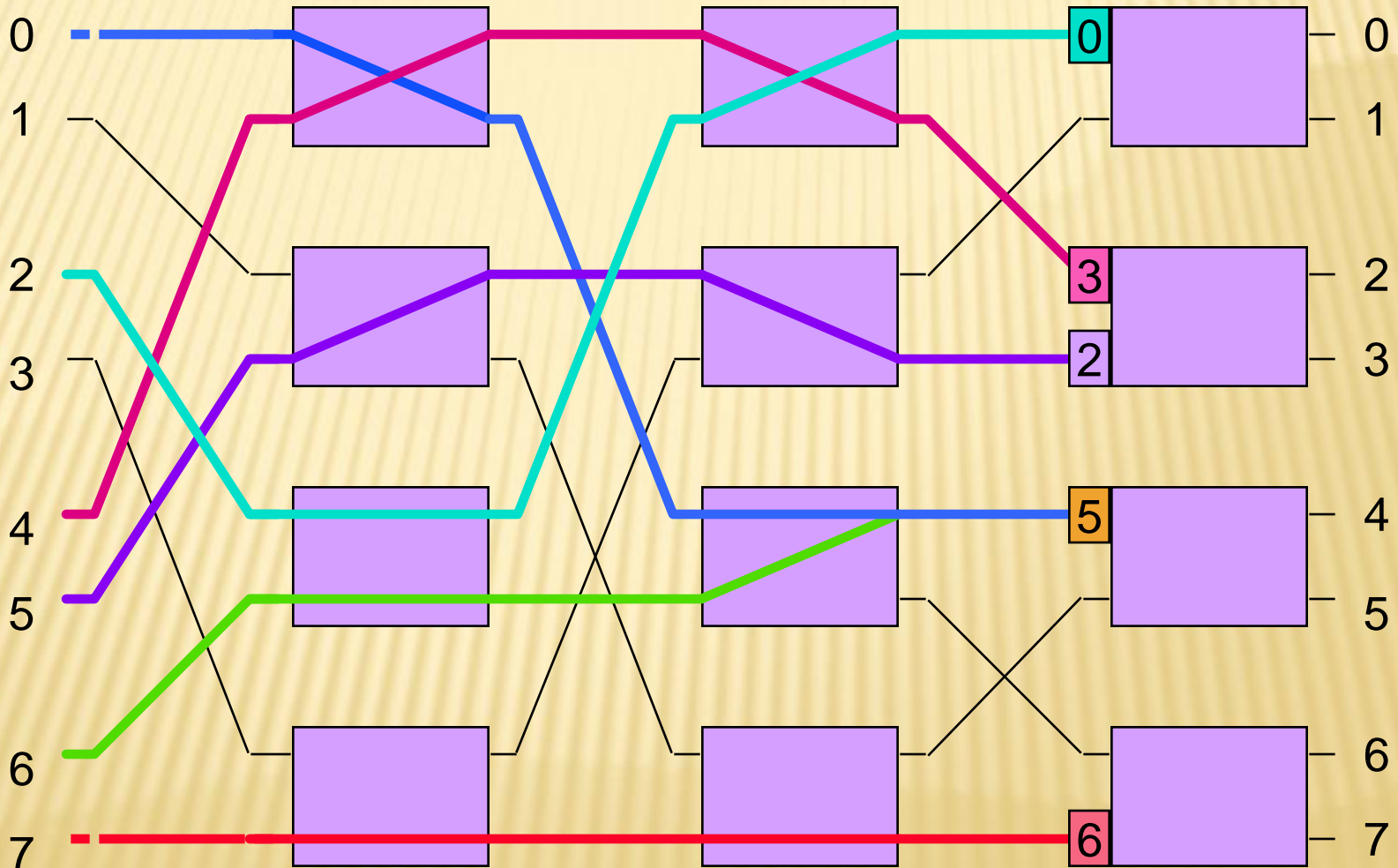
PERFORMANCE DEGRADATION



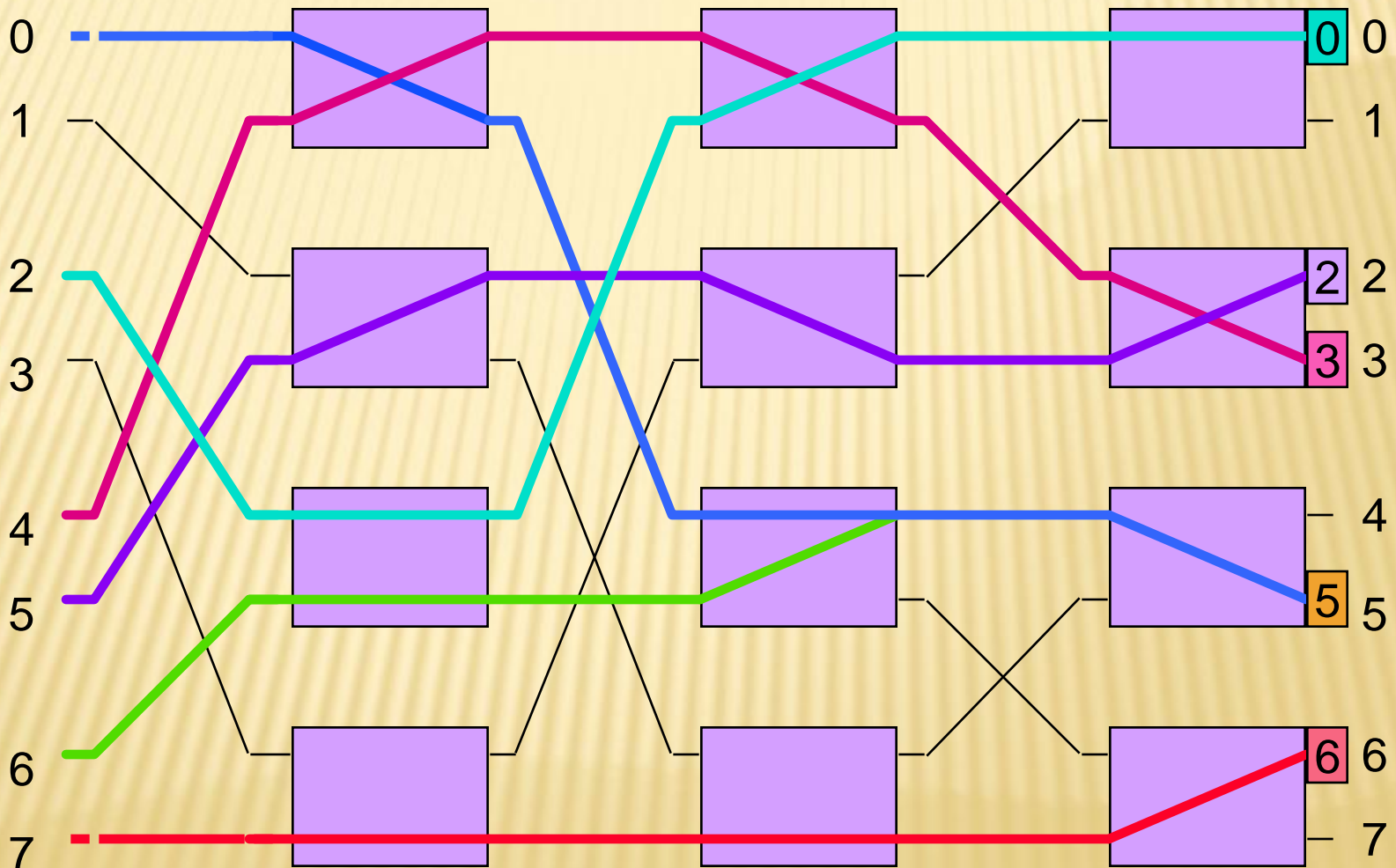
PERFORMANCE DEGRADATION



PERFORMANCE DEGRADATION



PERFORMANCE DEGRADATION



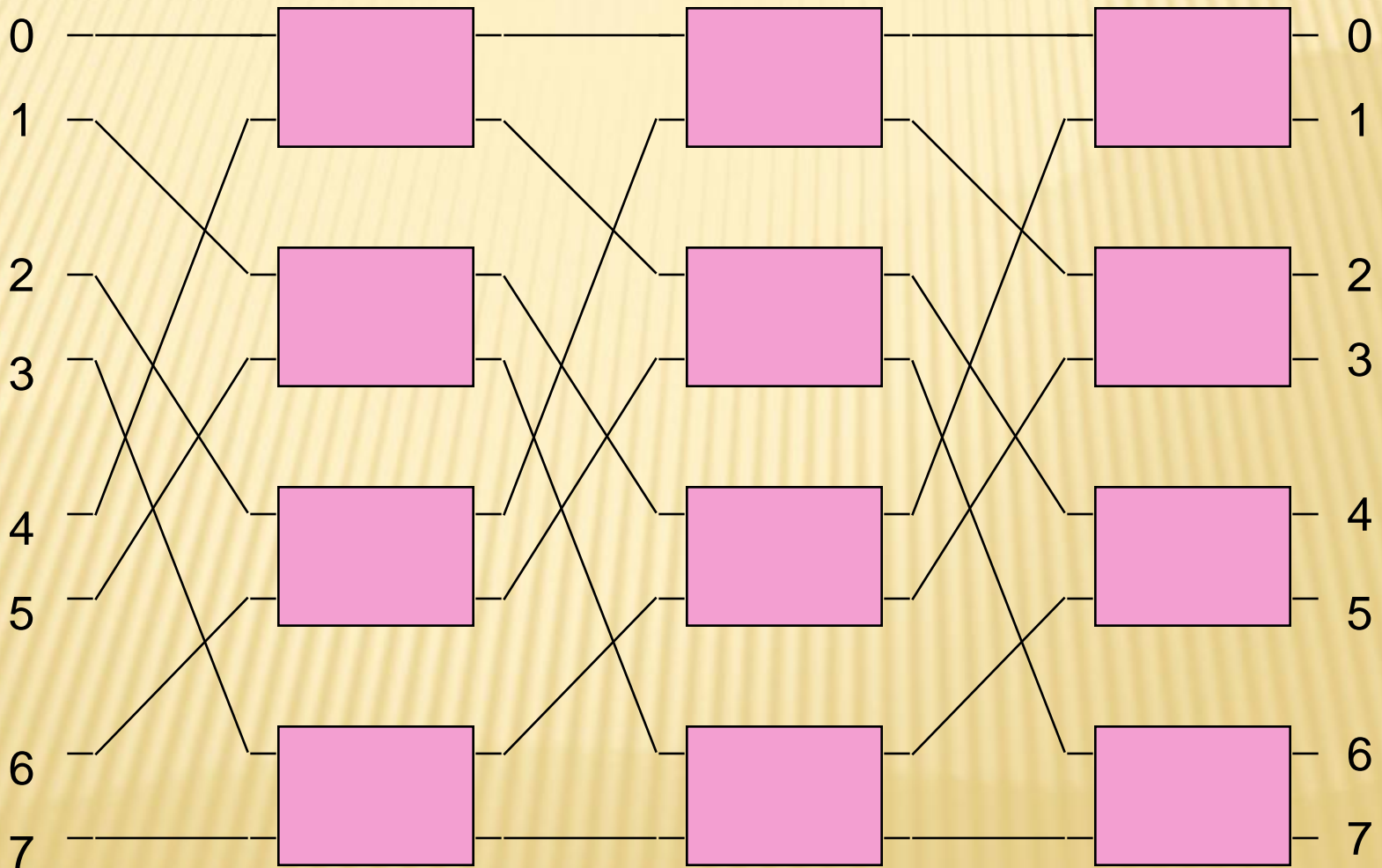
OMEGA NETWORK

- The omega network is another example of a banyan multistage interconnection network that can be used as a switch fabric
- The omega differs from the delta network in the pattern of interconnections between the stages
- The omega MIN uses the “perfect shuffle”

PERFECT SHUFFLE

- ✘ The interconnections between stages are defined by the logical “rotate left” of the bits used in the port ids
- ✘ Example: 000 ---> 000 ---> 000 ---> 000
- ✘ Example: 001 ---> 010 ---> 100 ---> 001
- ✘ Example: 011 ---> 110 ---> 101 ---> 011
- ✘ Example: 111 ---> 111 ---> 111 ---> 111

8 X 8 OMEGA NETWORK

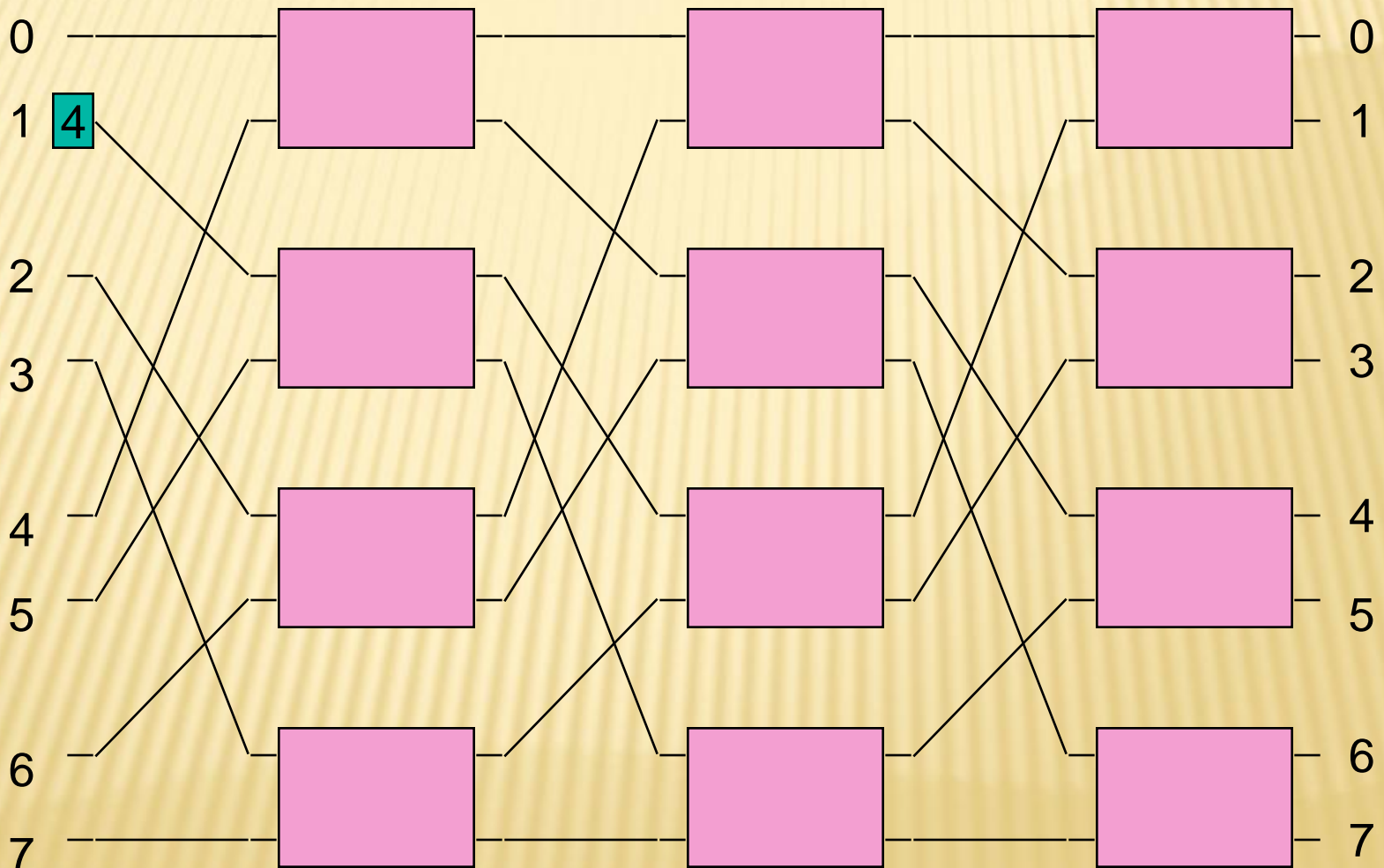


SELF ROUTING

- Omega network has self-routing property
- The path for a cell to reach its destination can be determined directly from its routing tag (i.e., destination port id)
- Stage k of the MIN looks at bit k of the tag
- If bit k is 0, then send cell out upper port
- If bit k is 1, then send cell out lower port
- Works for every possible input port (really!)

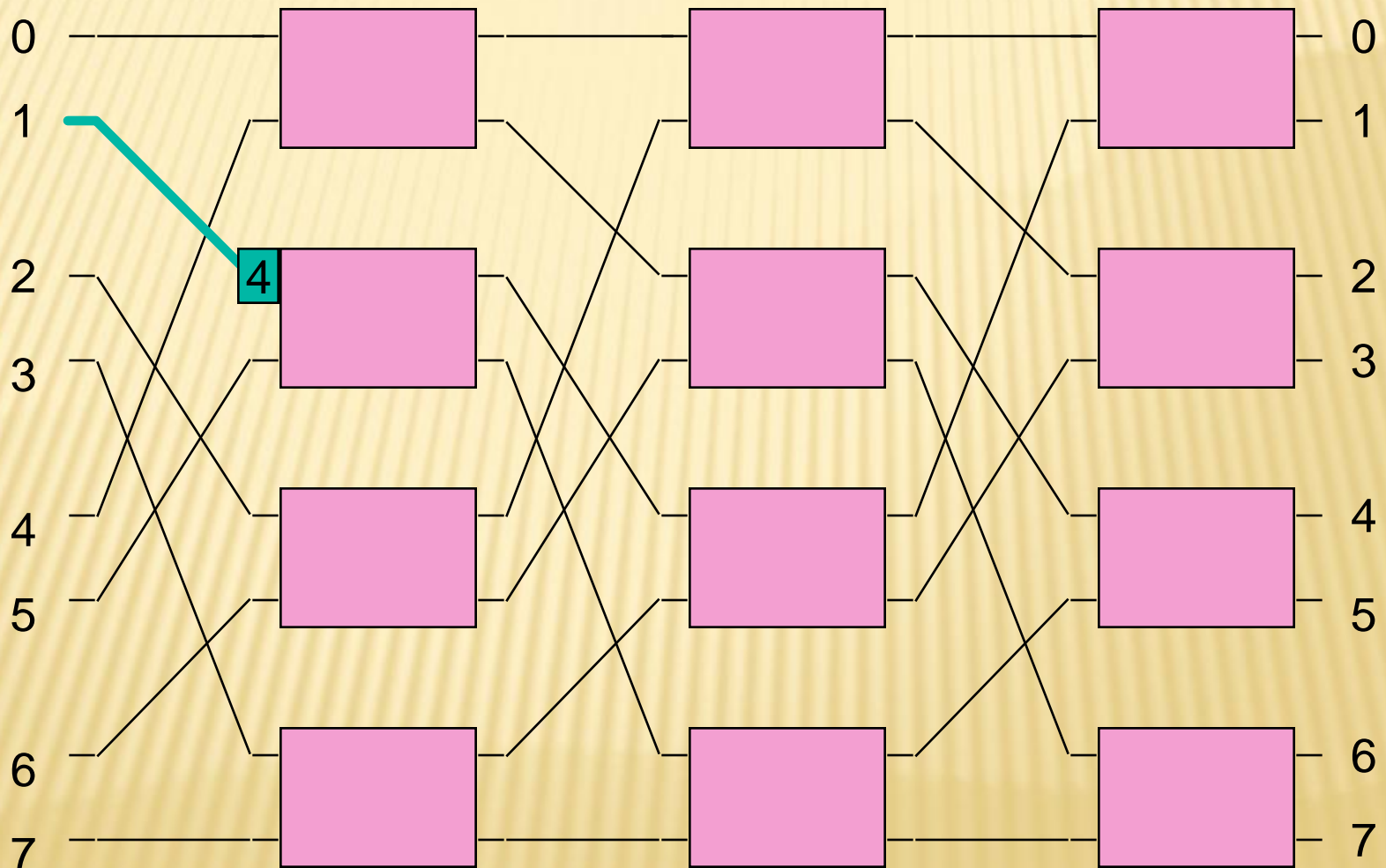
Example of Self Routing

Cell destined for output port 4 ($= 100_2$)



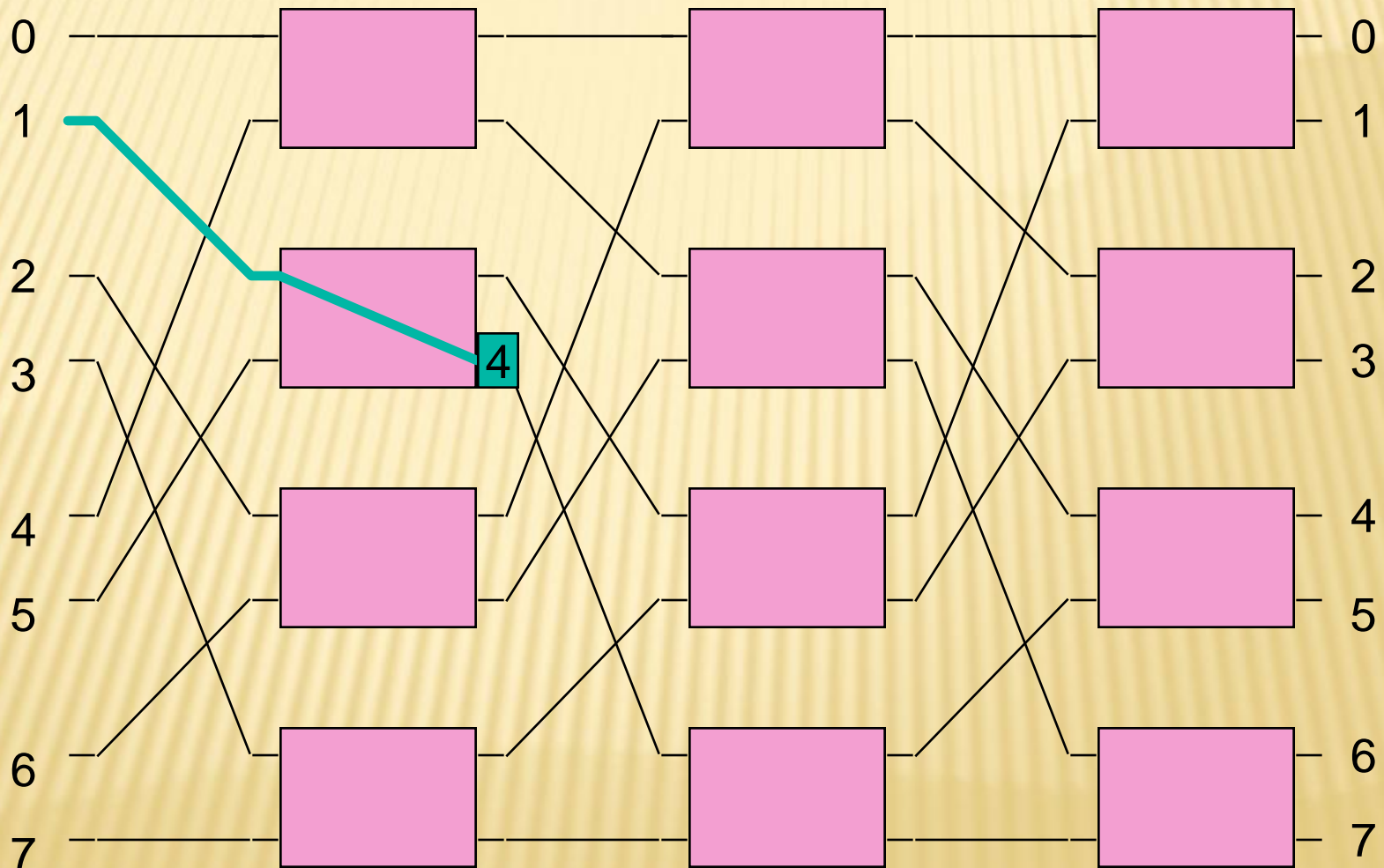
Example of Self Routing

Cell destined for output port 4 ($= 100_2$)



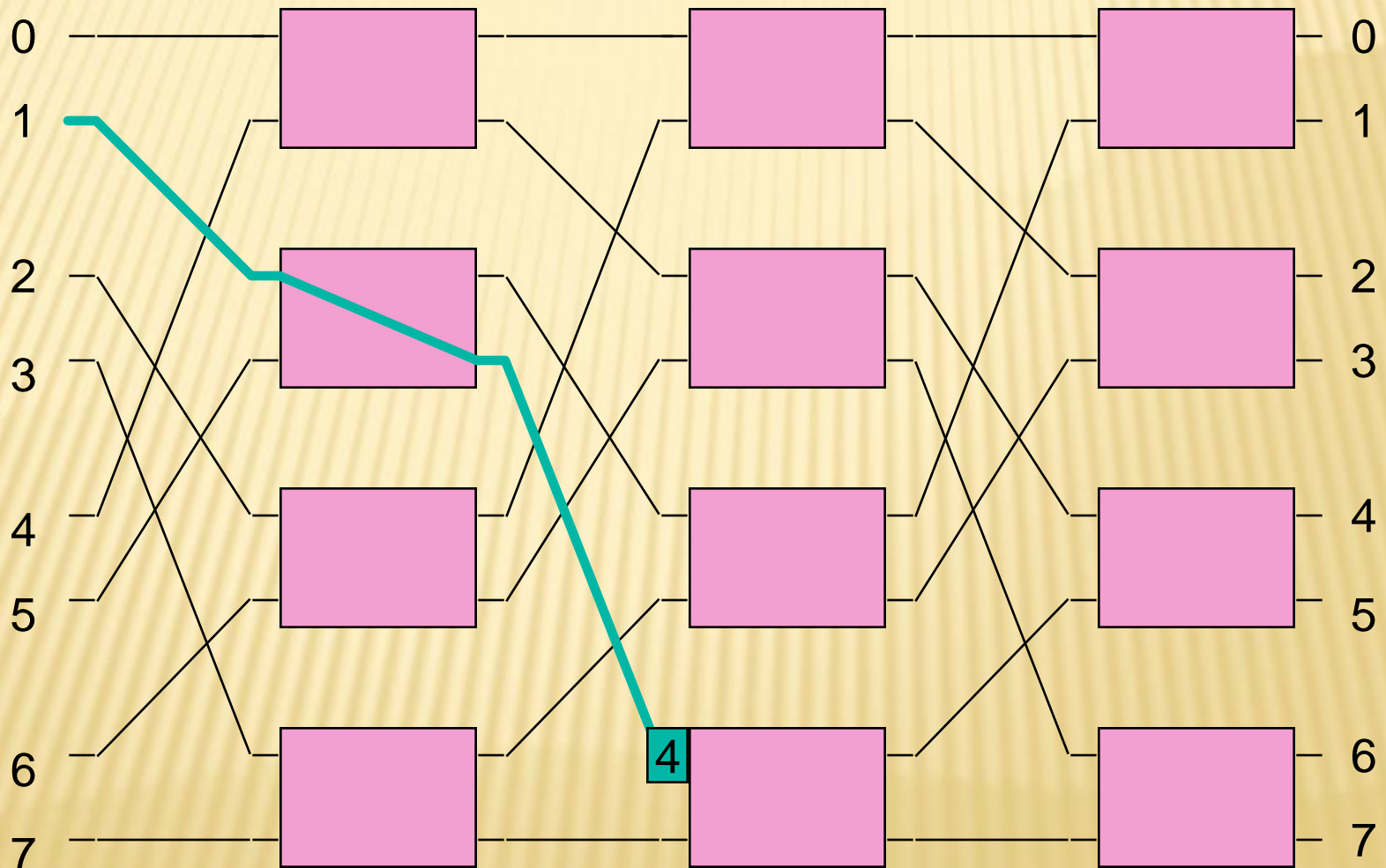
Example of Self Routing

Cell destined for output port 4 ($= 100_2$)



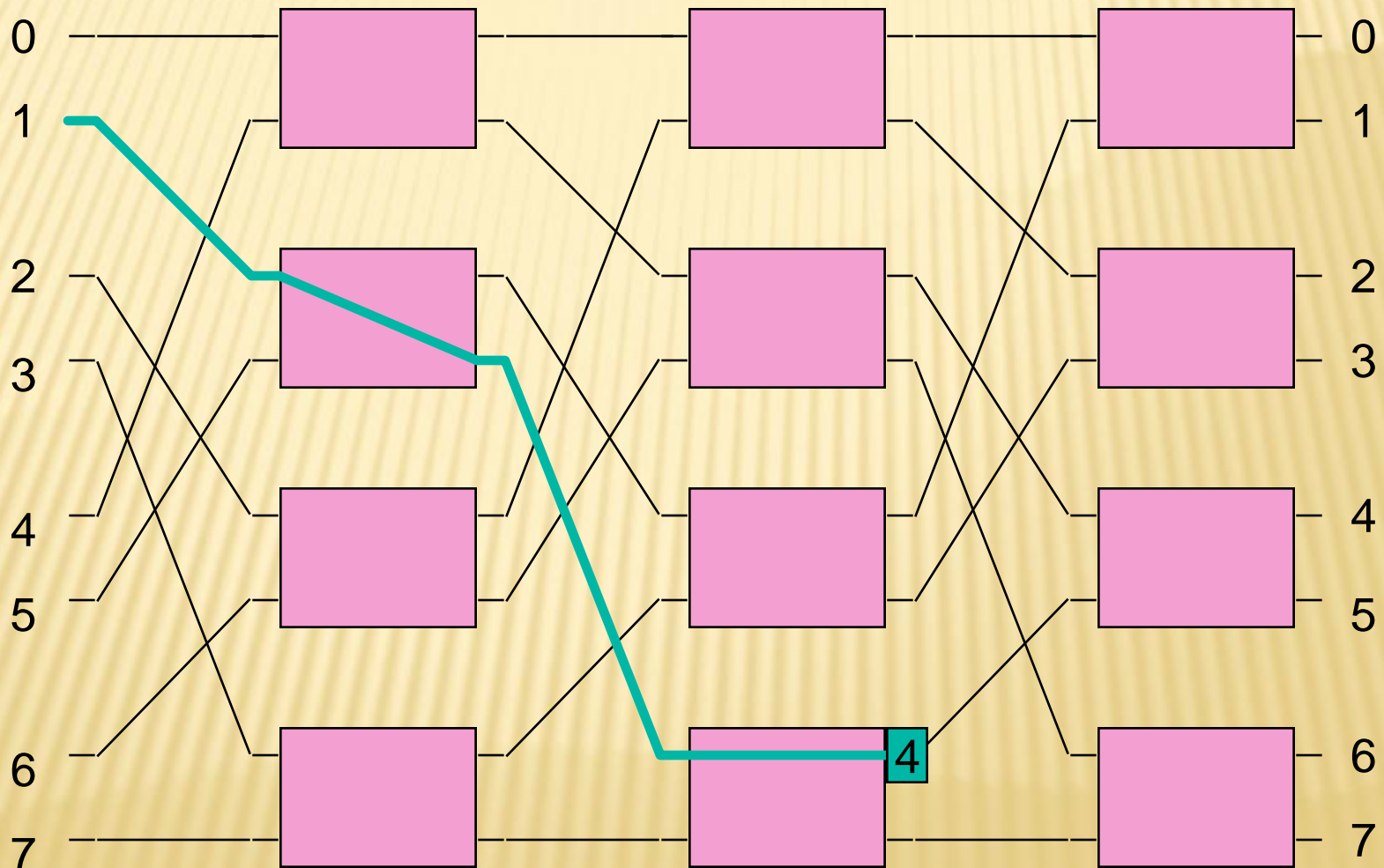
Example of Self Routing

Cell destined for output port 4 ($= 100_2$)



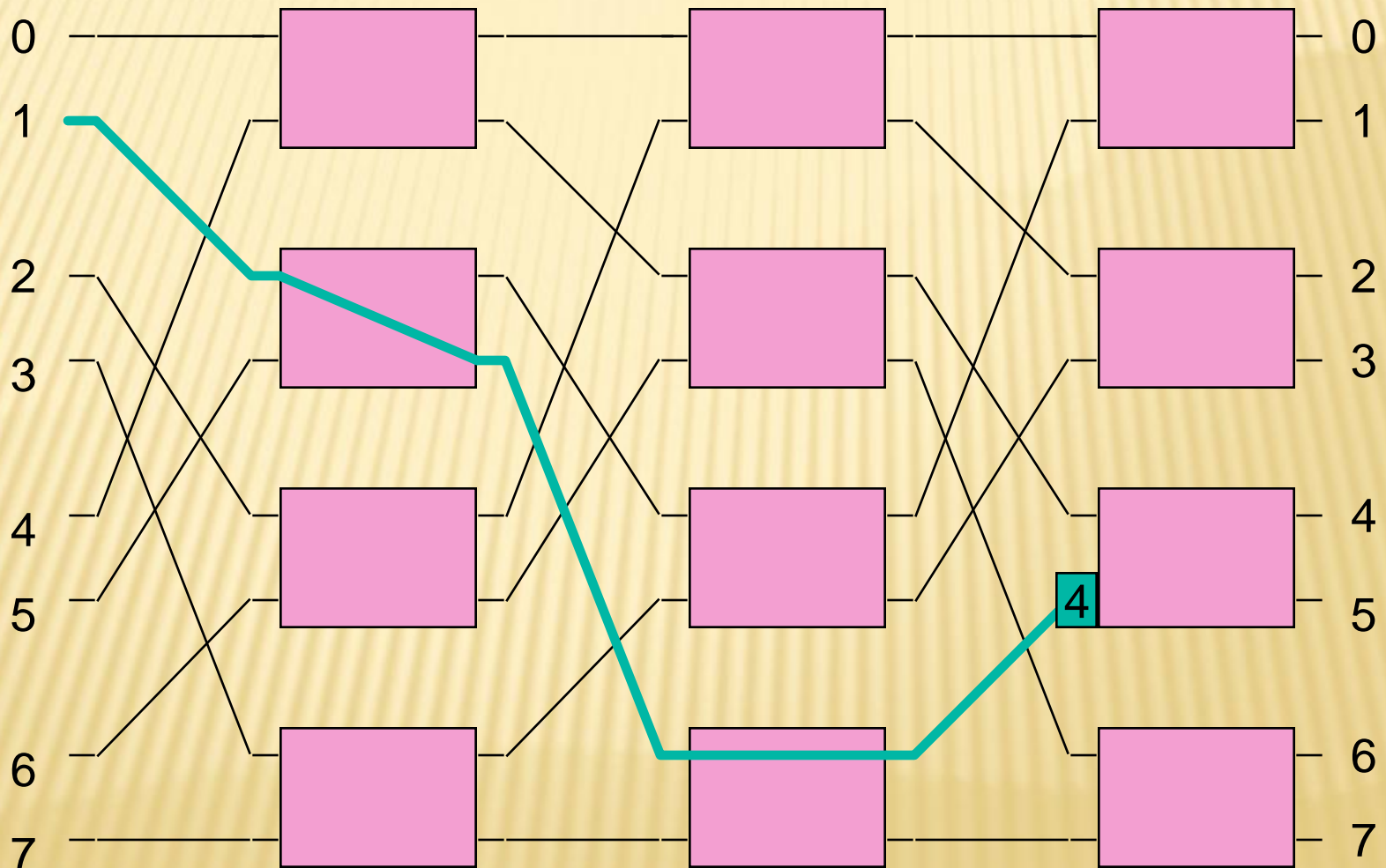
Example of Self Routing

Cell destined for output port 4 ($= 100_2$)



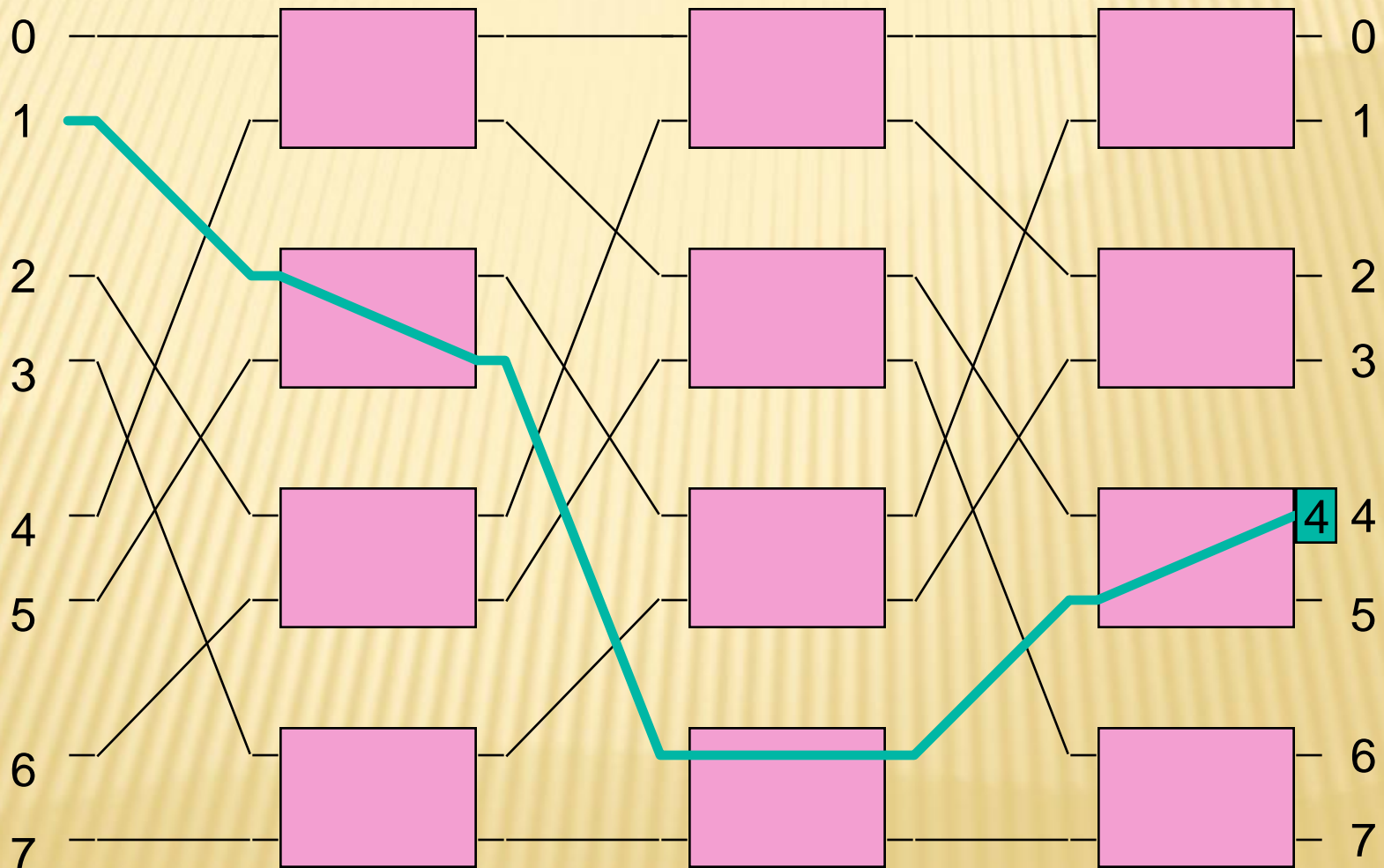
Example of Self Routing

Cell destined for output port 4 ($= 100_2$)



Example of Self Routing

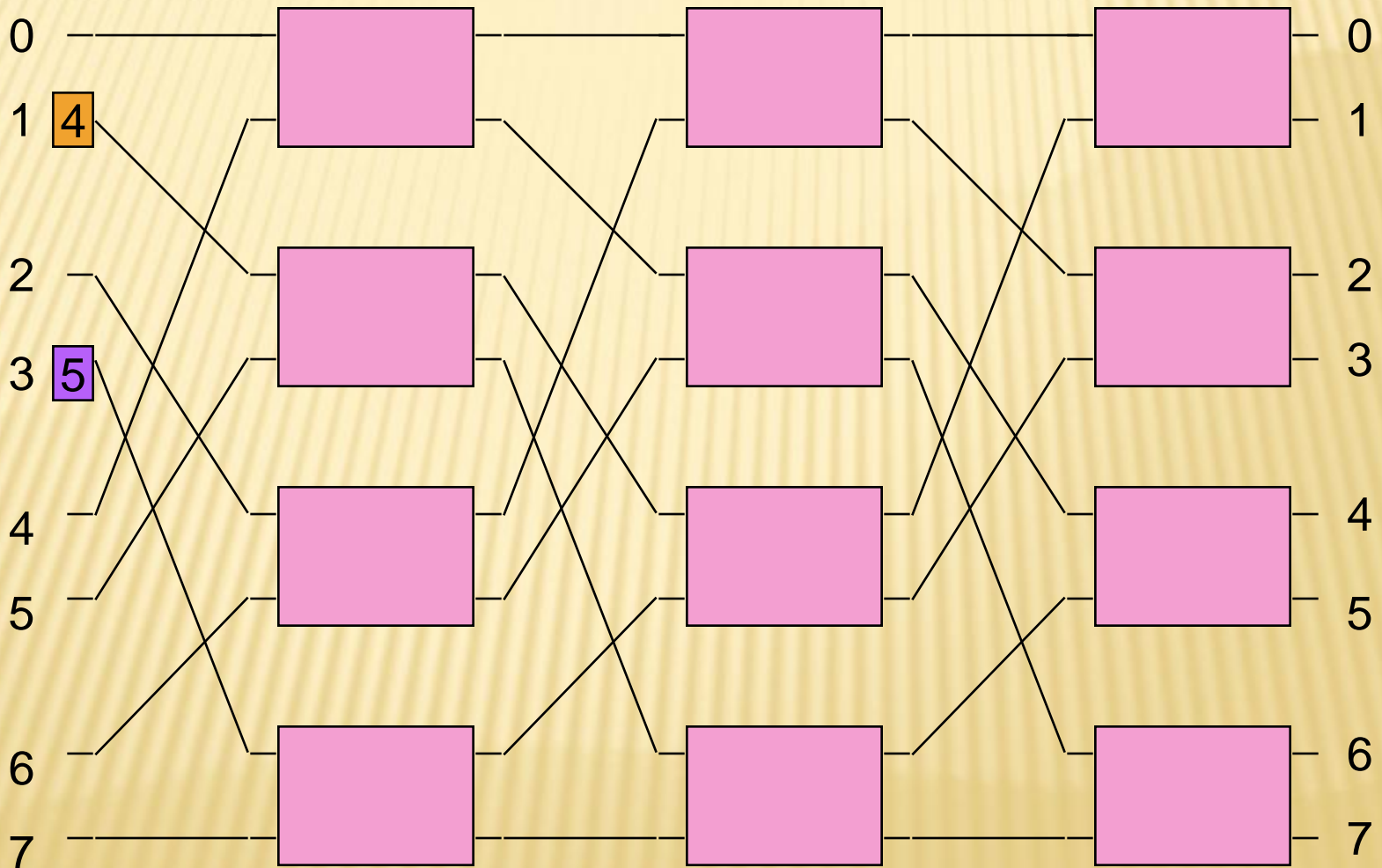
Cell destined for output port 4 ($= 100_2$)



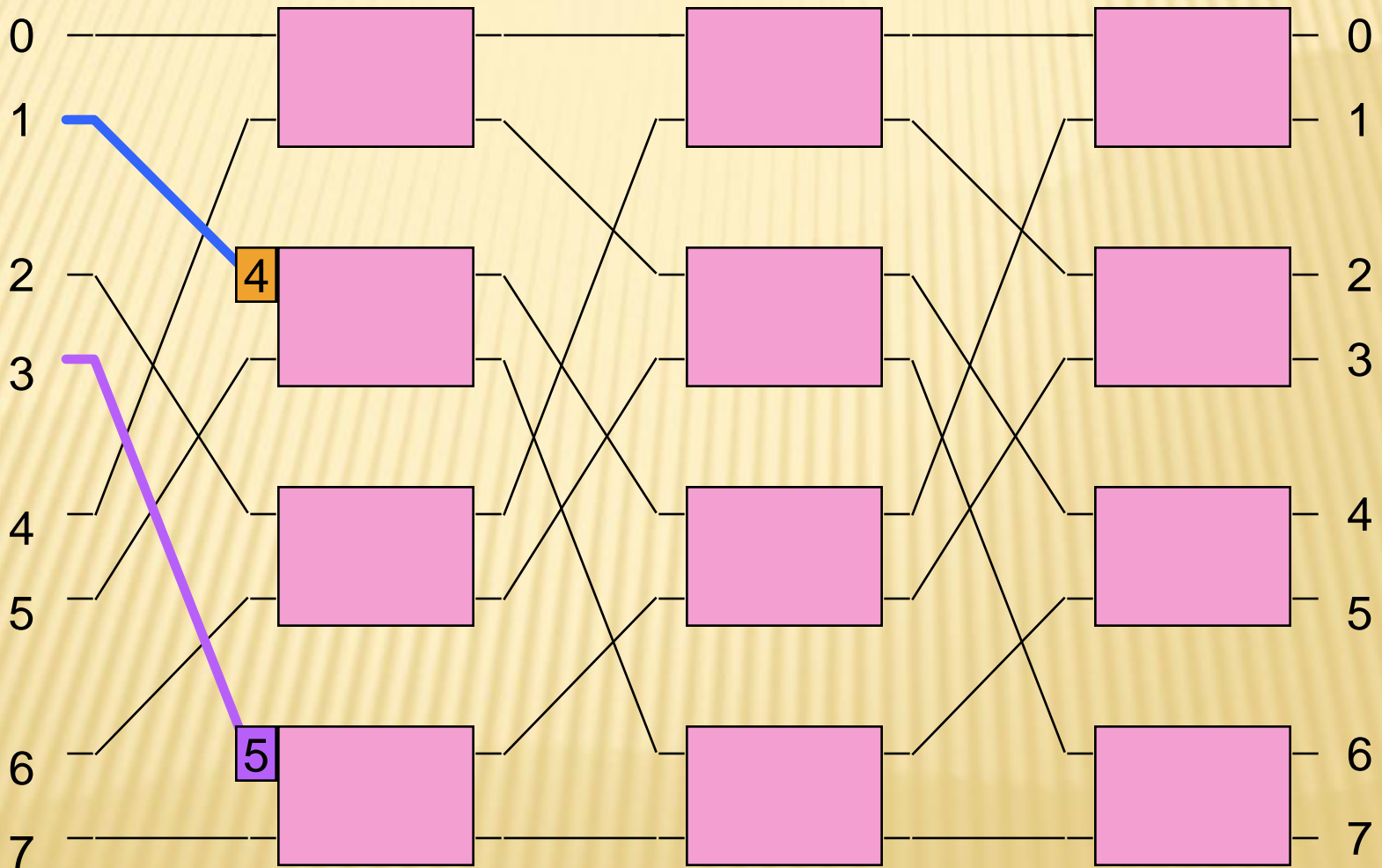
PATH CONTENTION

- ✘ The omega network has the problems as the delta network with output port contention and path contention
- ✘ Again, the result in a bufferless switch fabric is cell loss (one cell wins, one loses)
- ✘ Path contention and output port contention can seriously degrade the achievable throughput of the switch

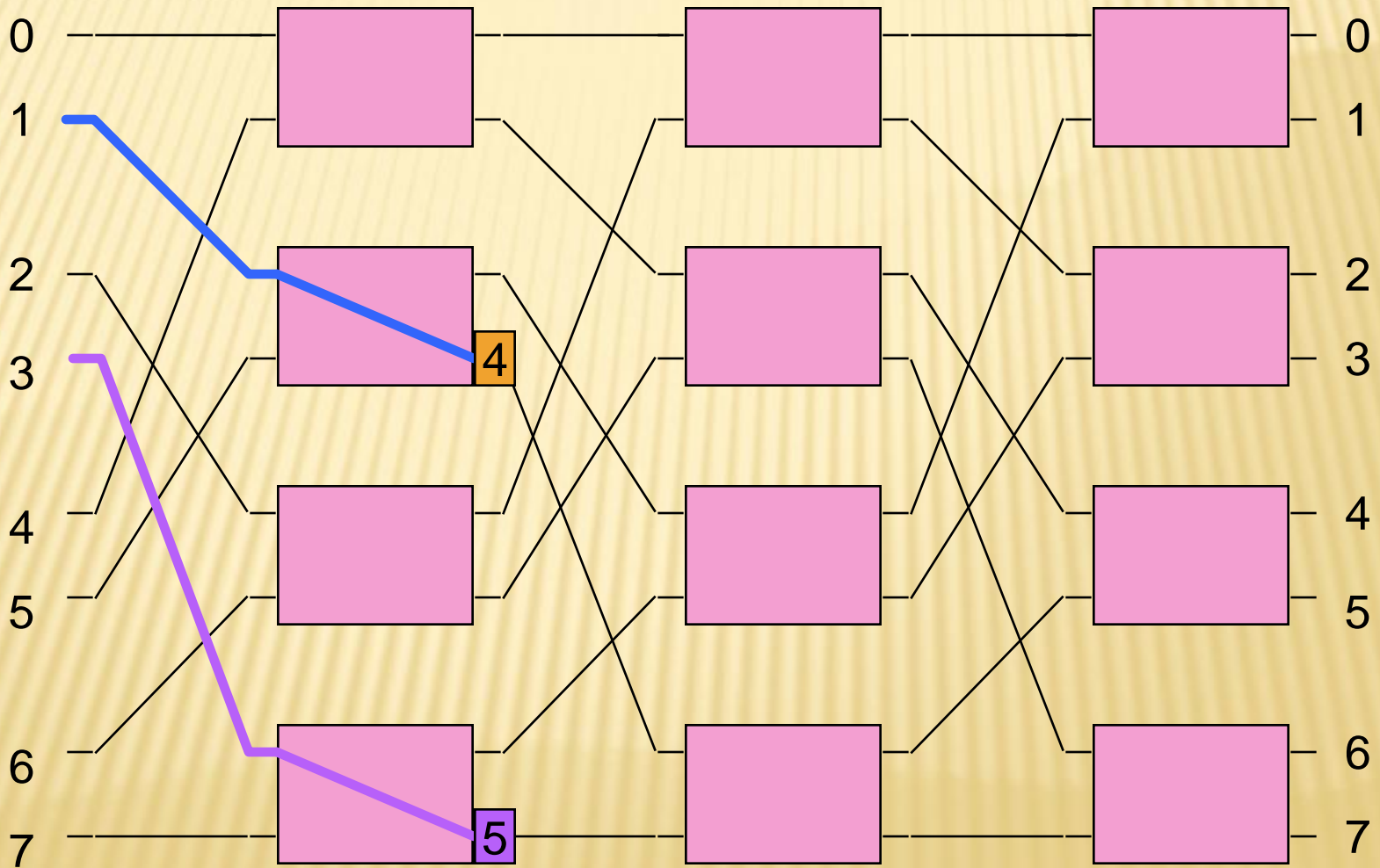
Path Contention



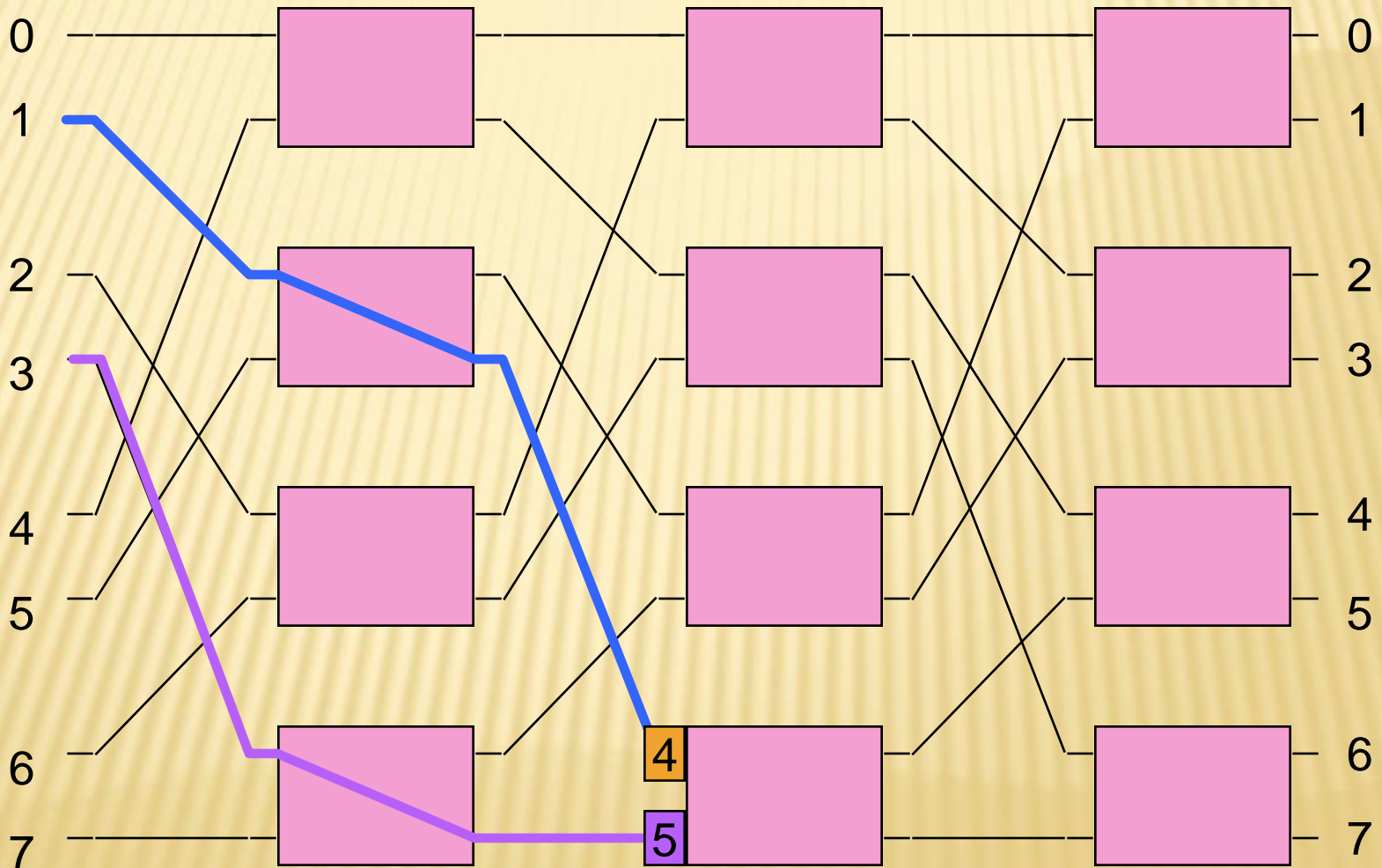
Path Contention



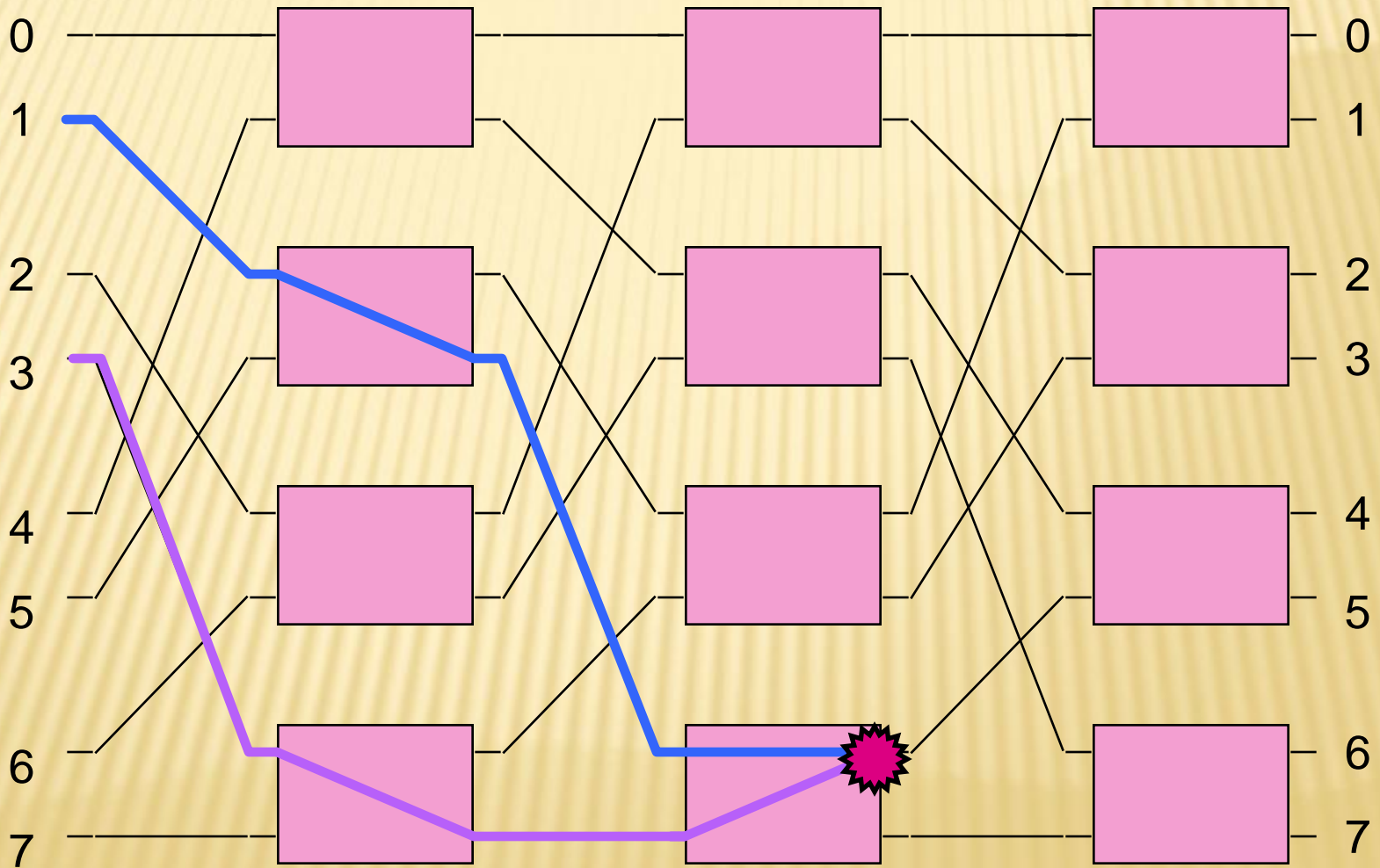
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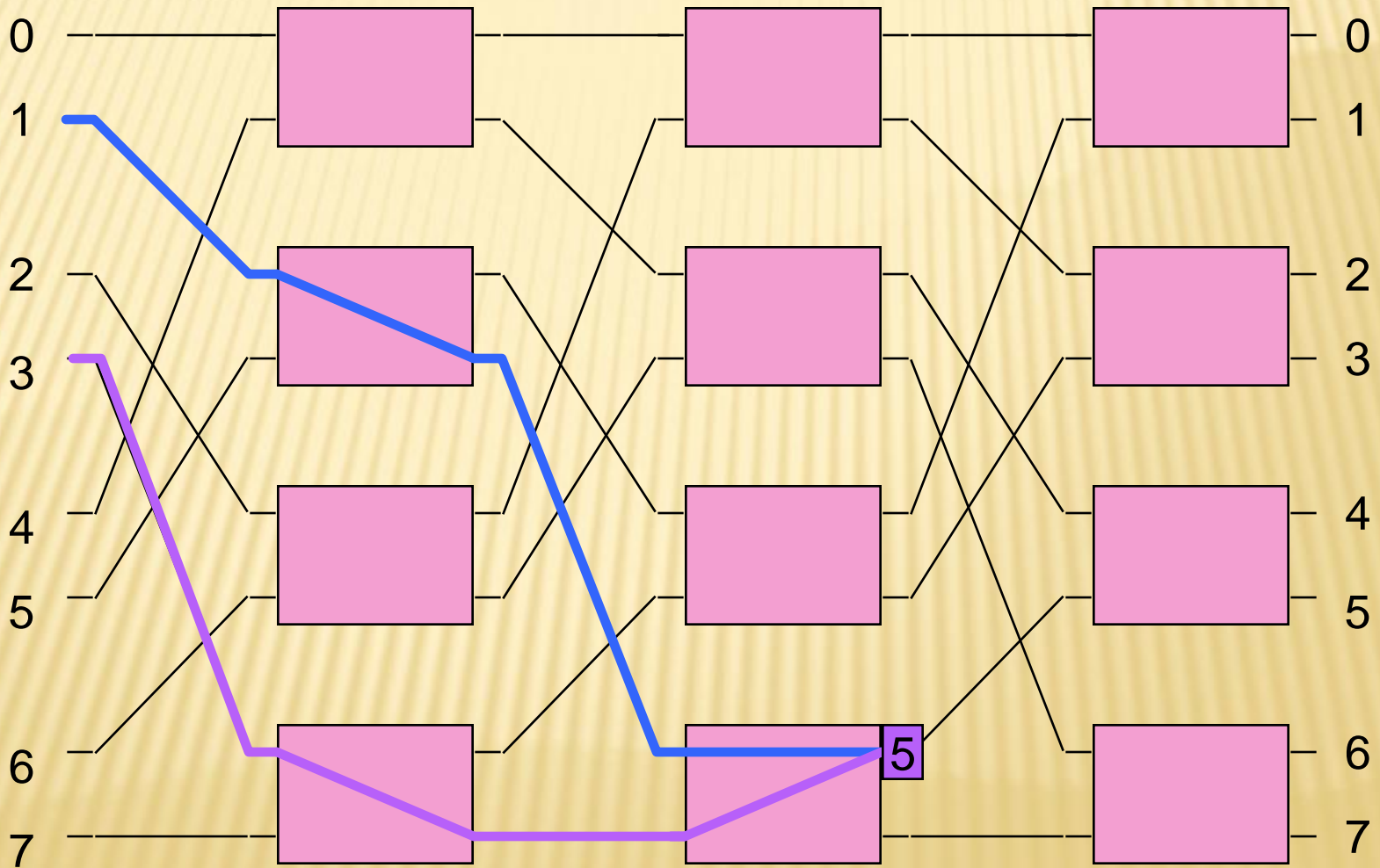
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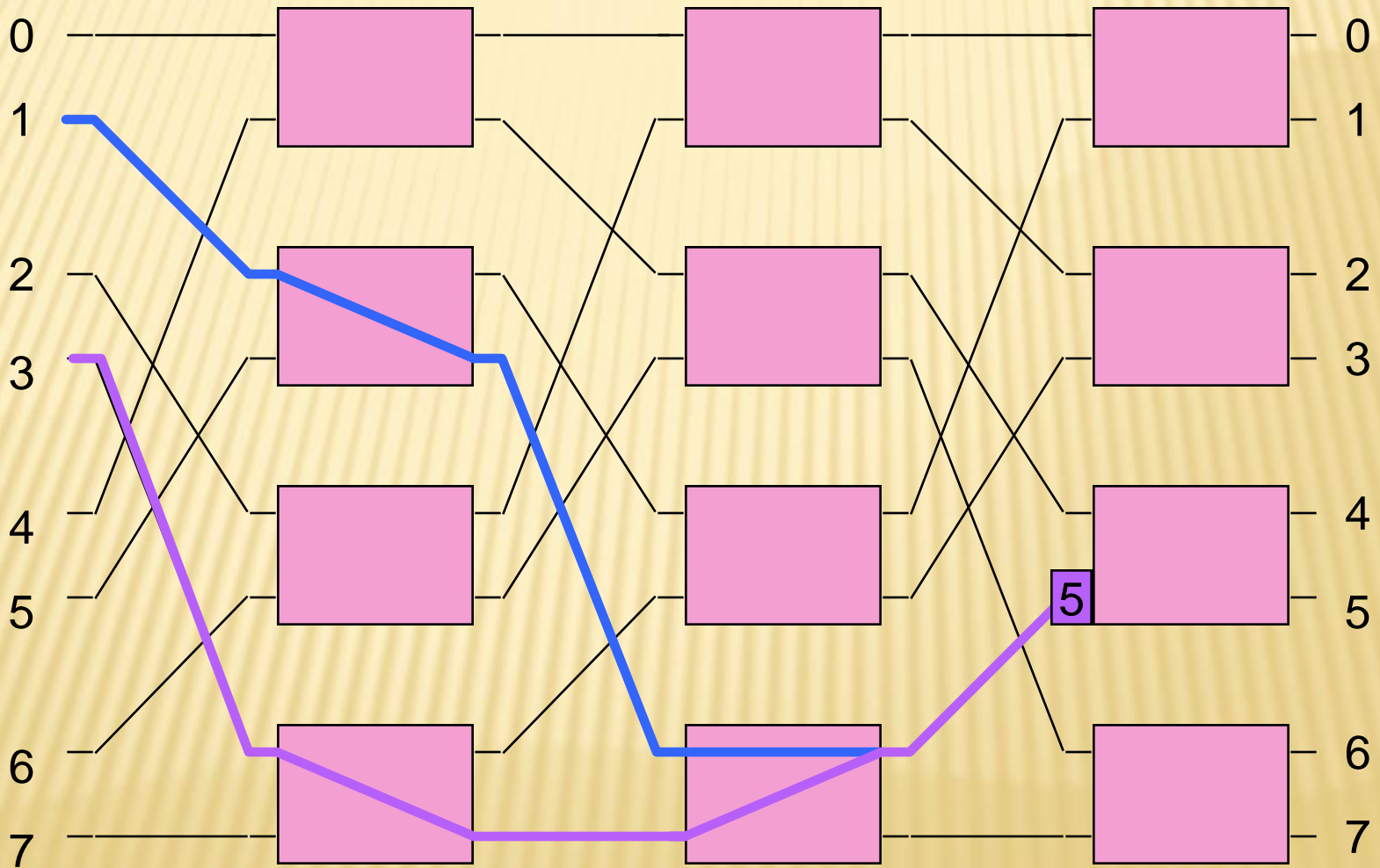
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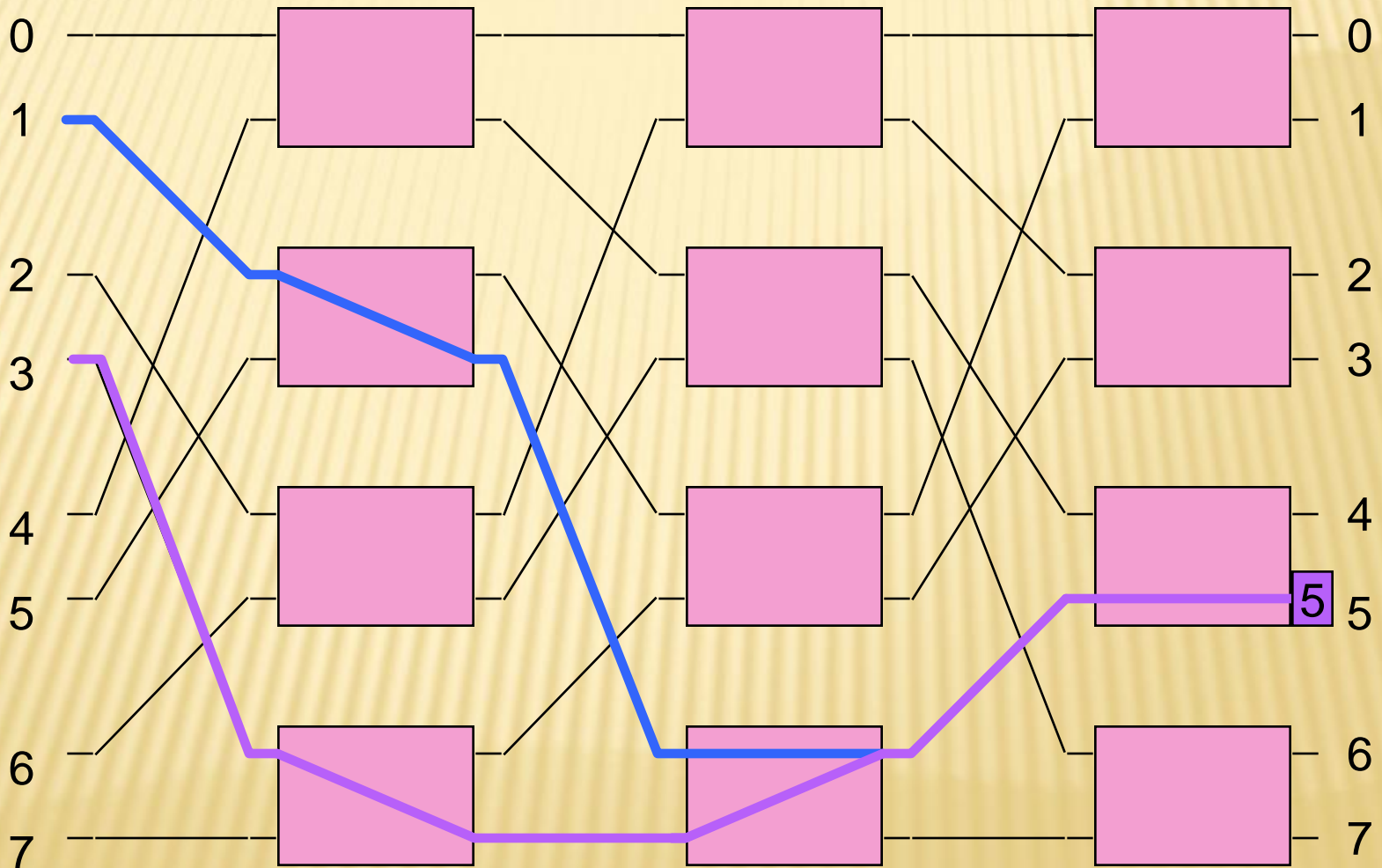
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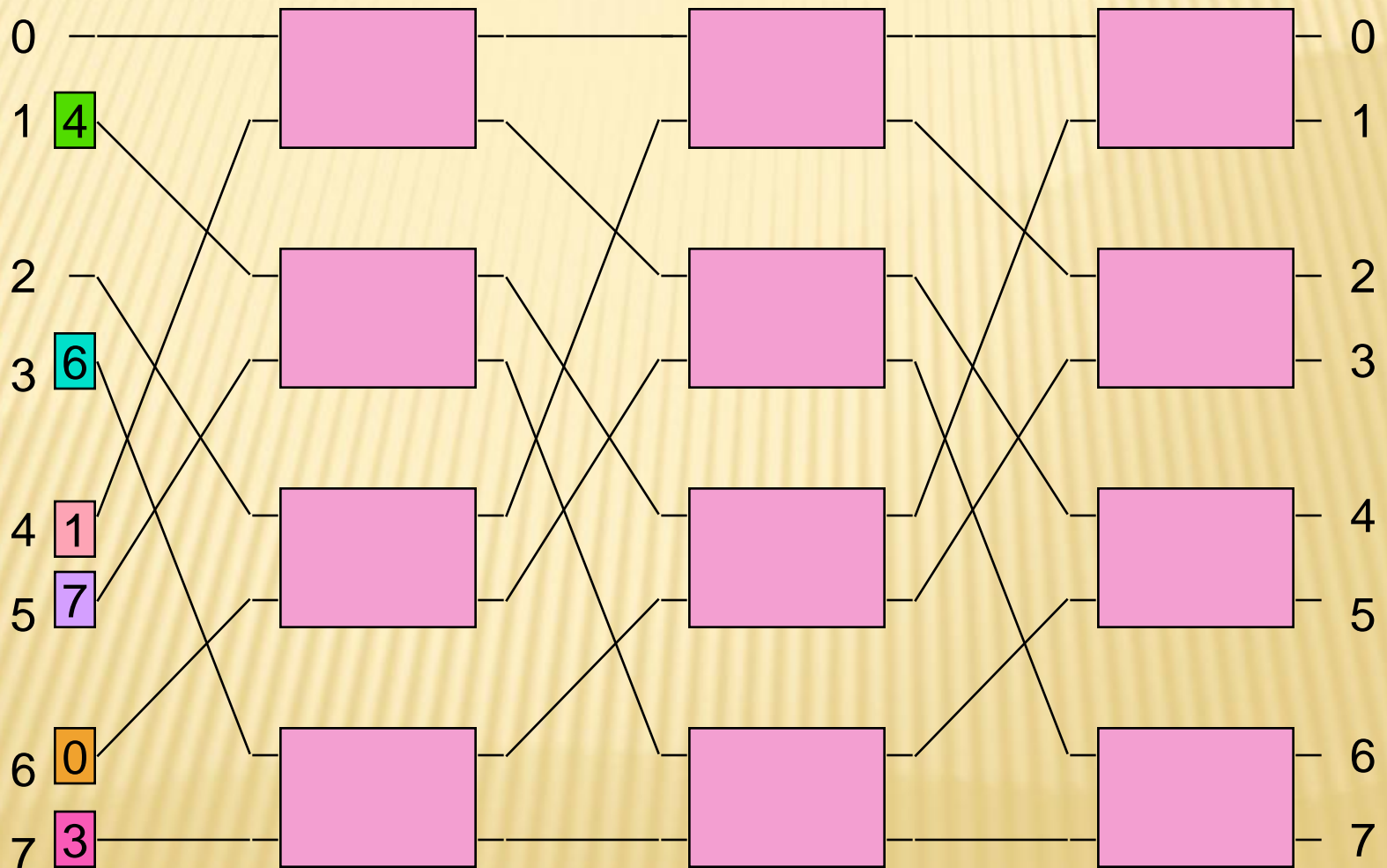
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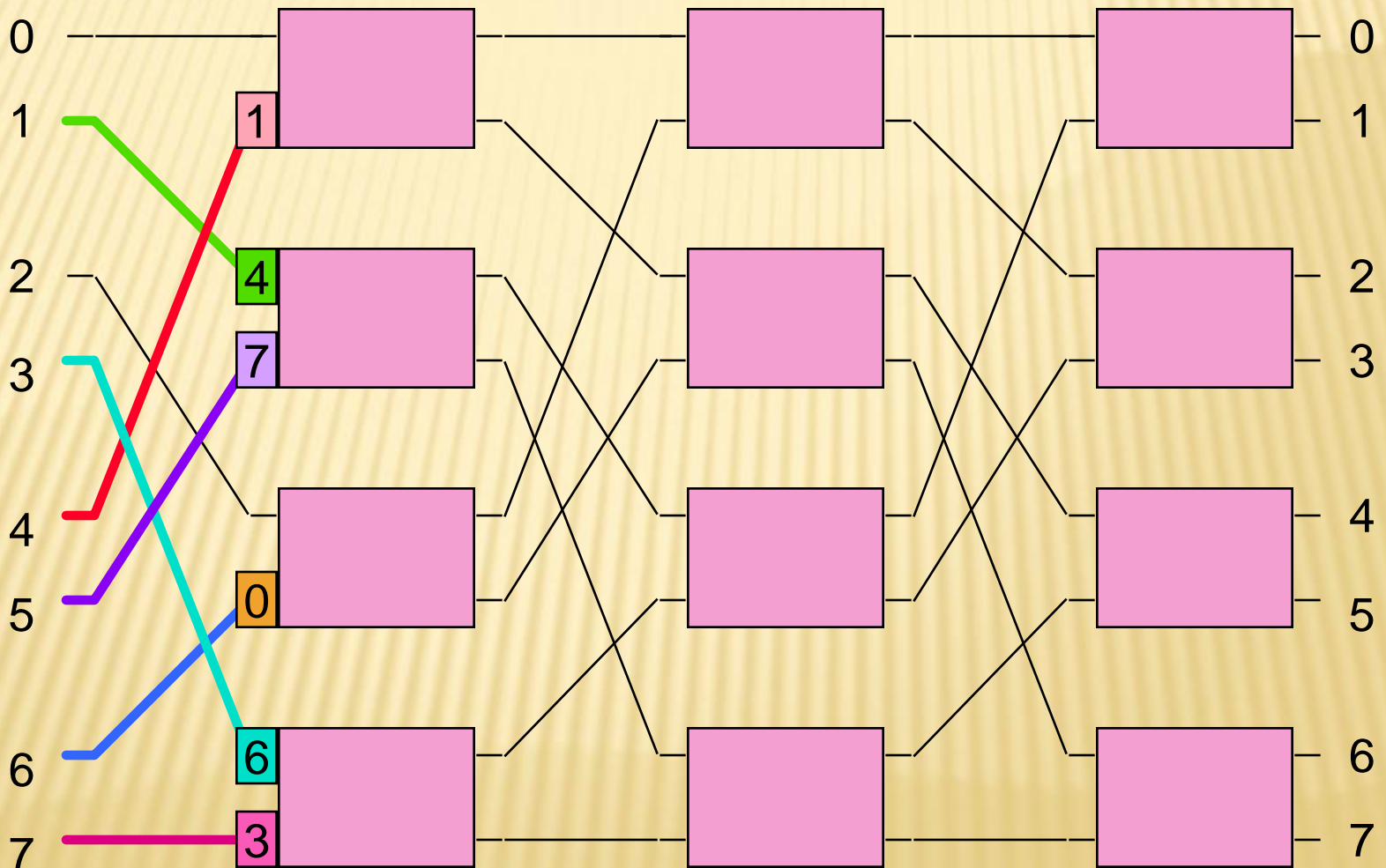
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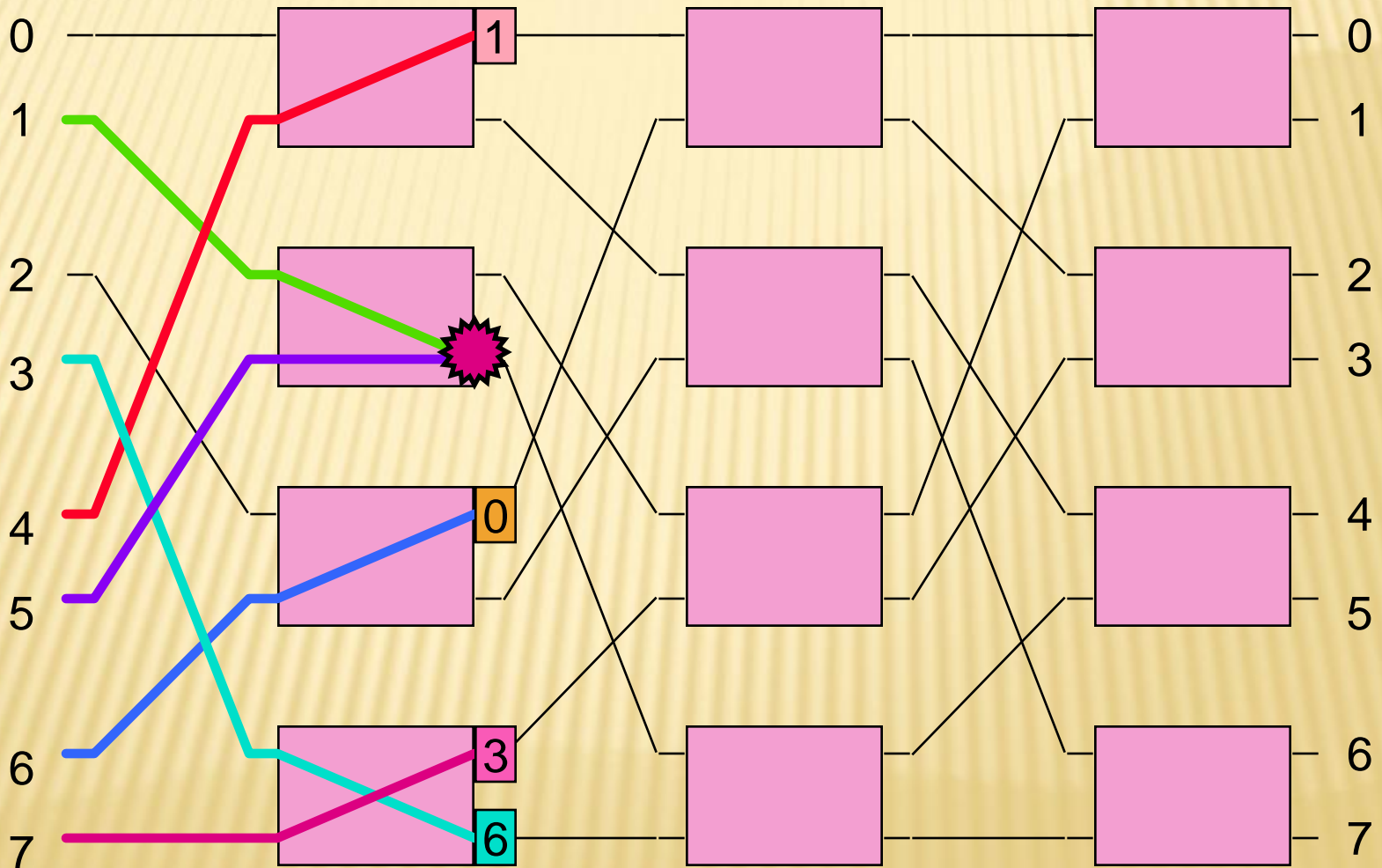
PERFORMANCE DEGRADATION



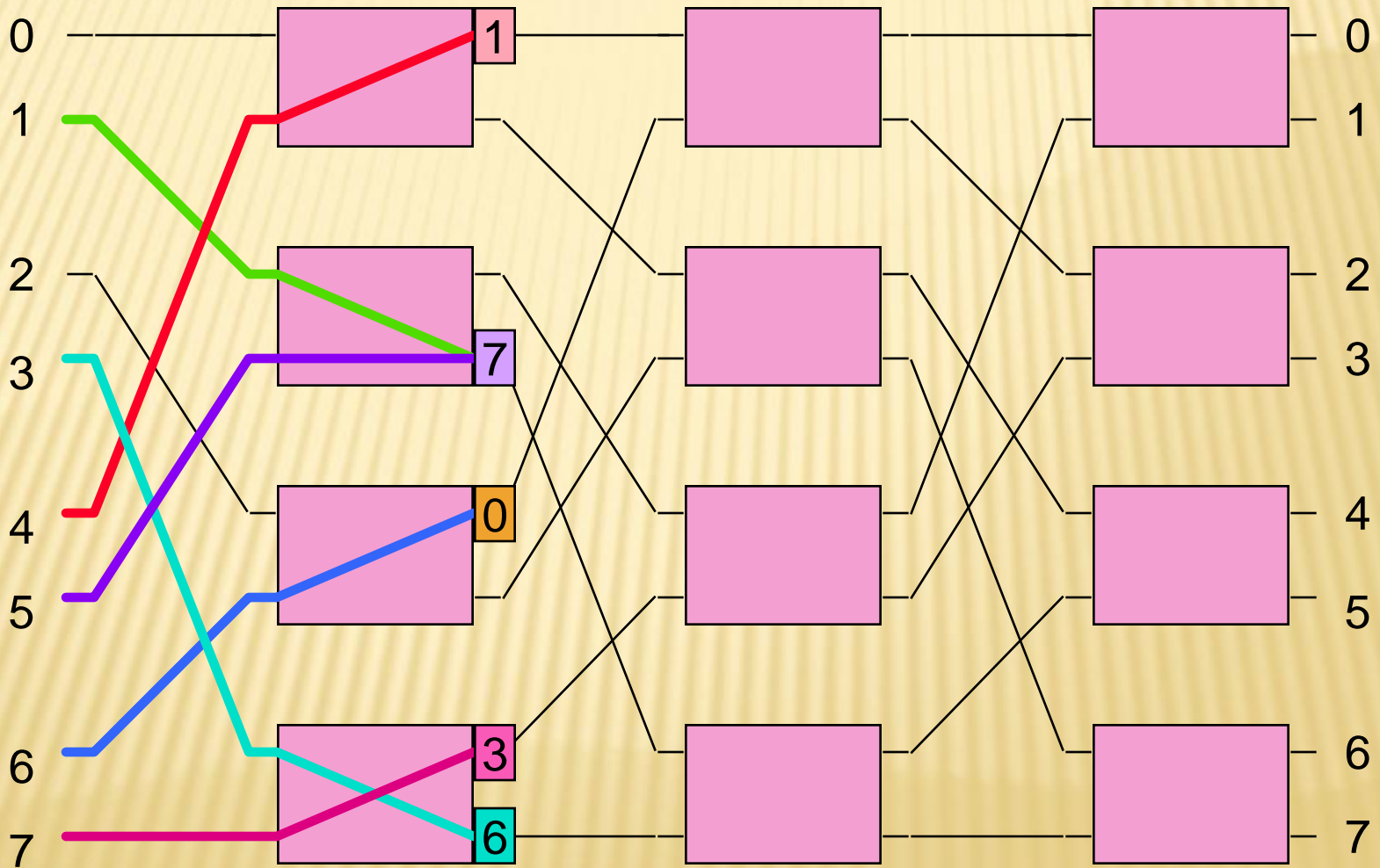
PERFORMANCE DEGRADATION



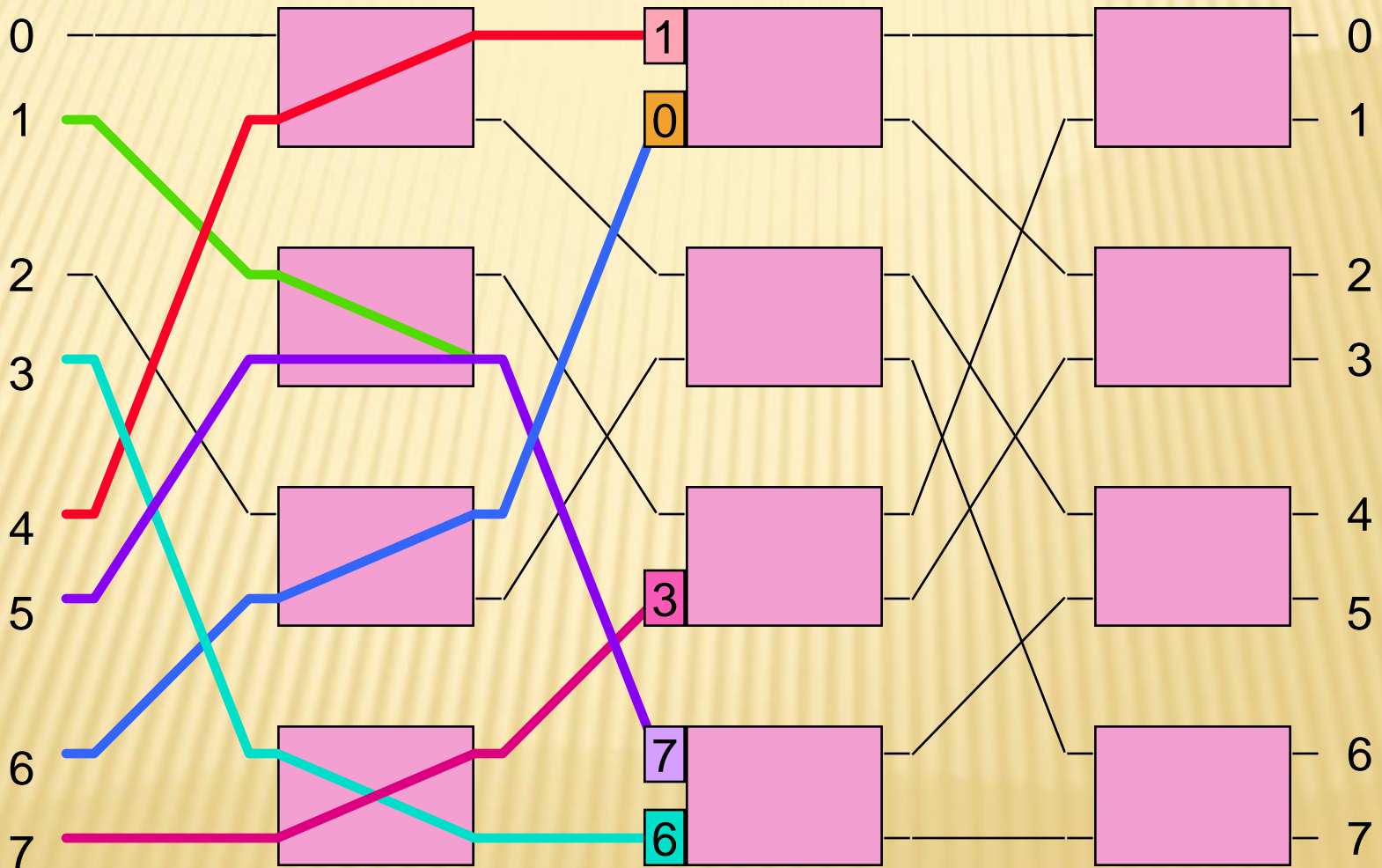
PERFORMANCE DEGRADATION



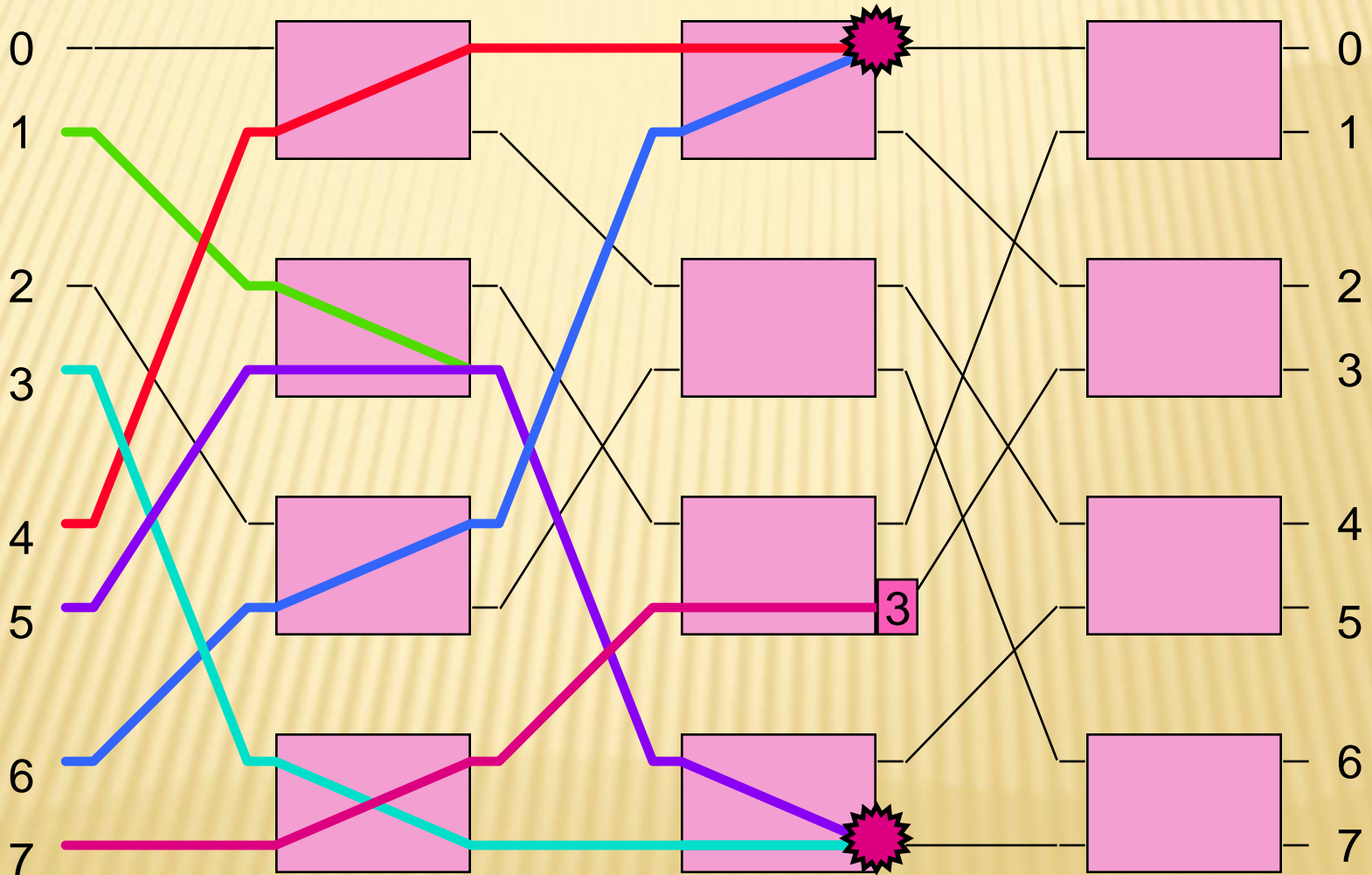
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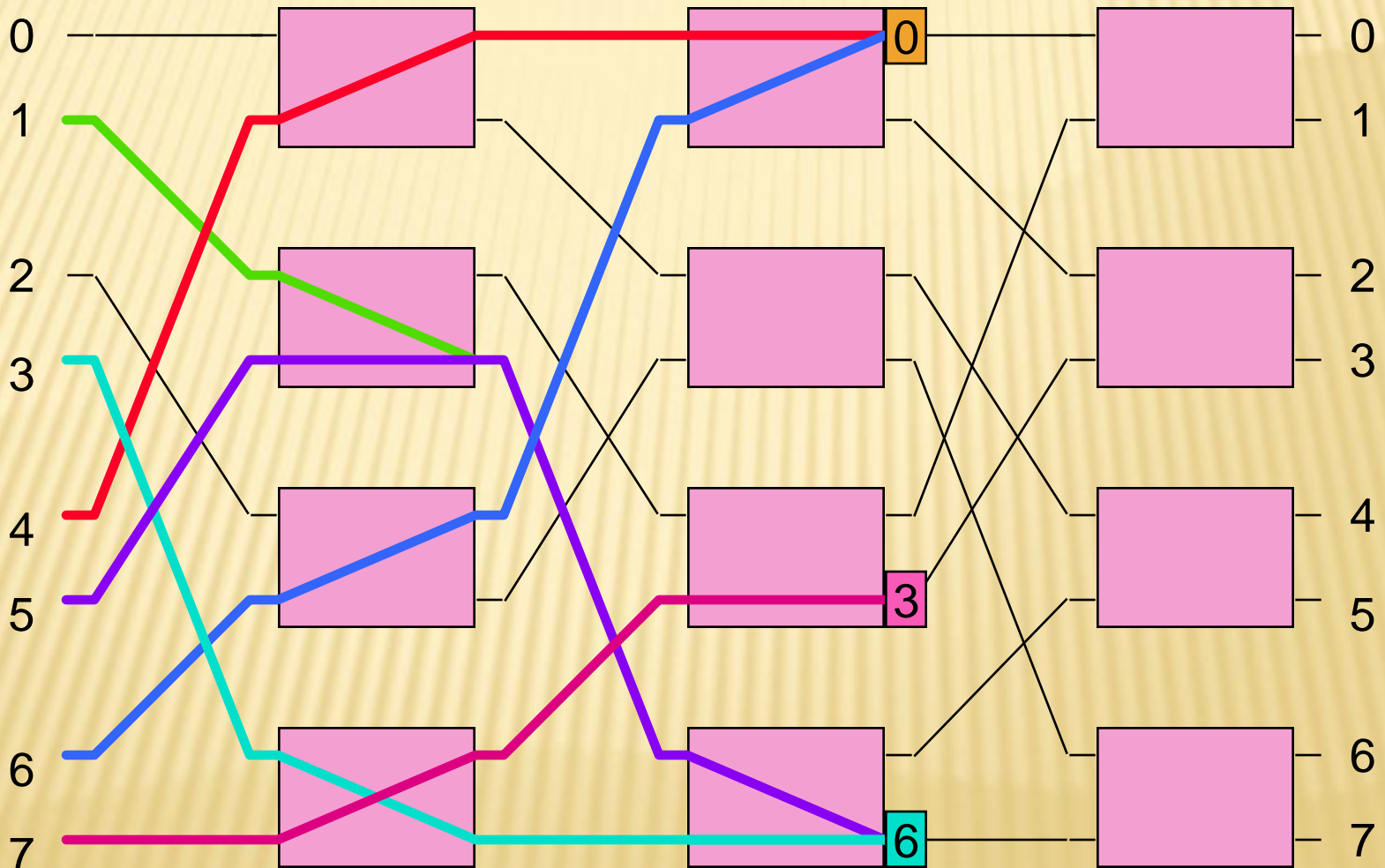
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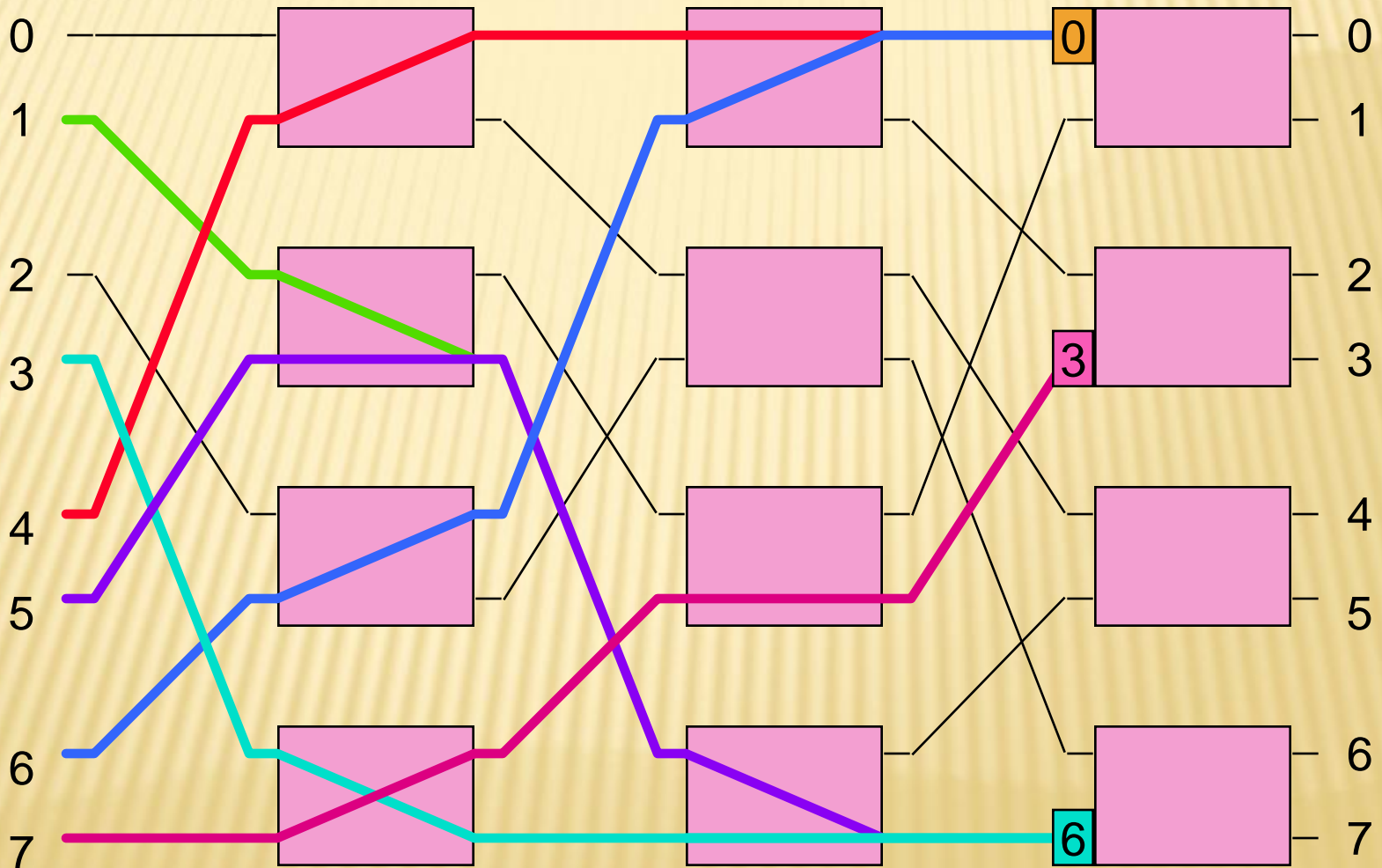
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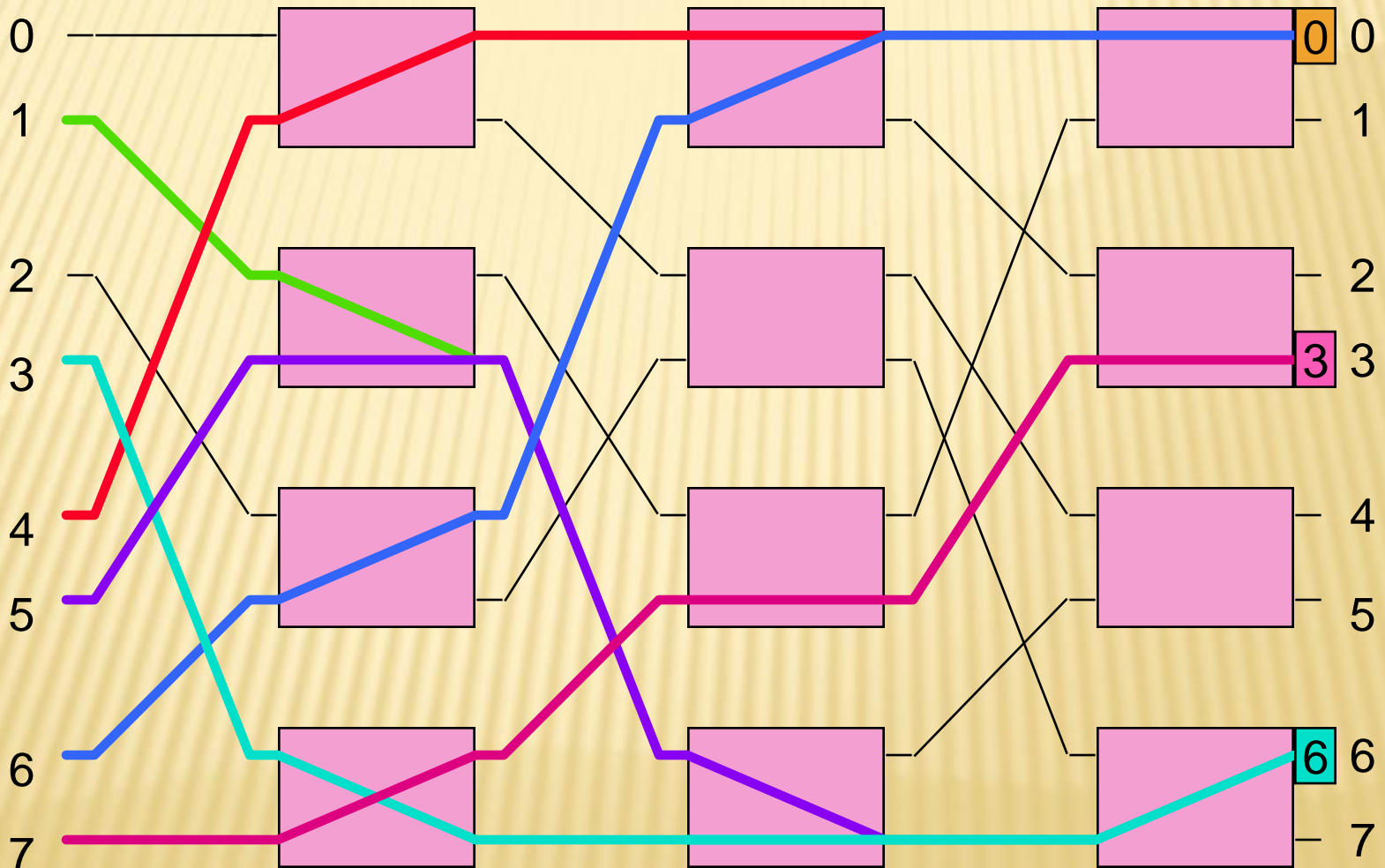
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PERFORMANCE DEGRADATION



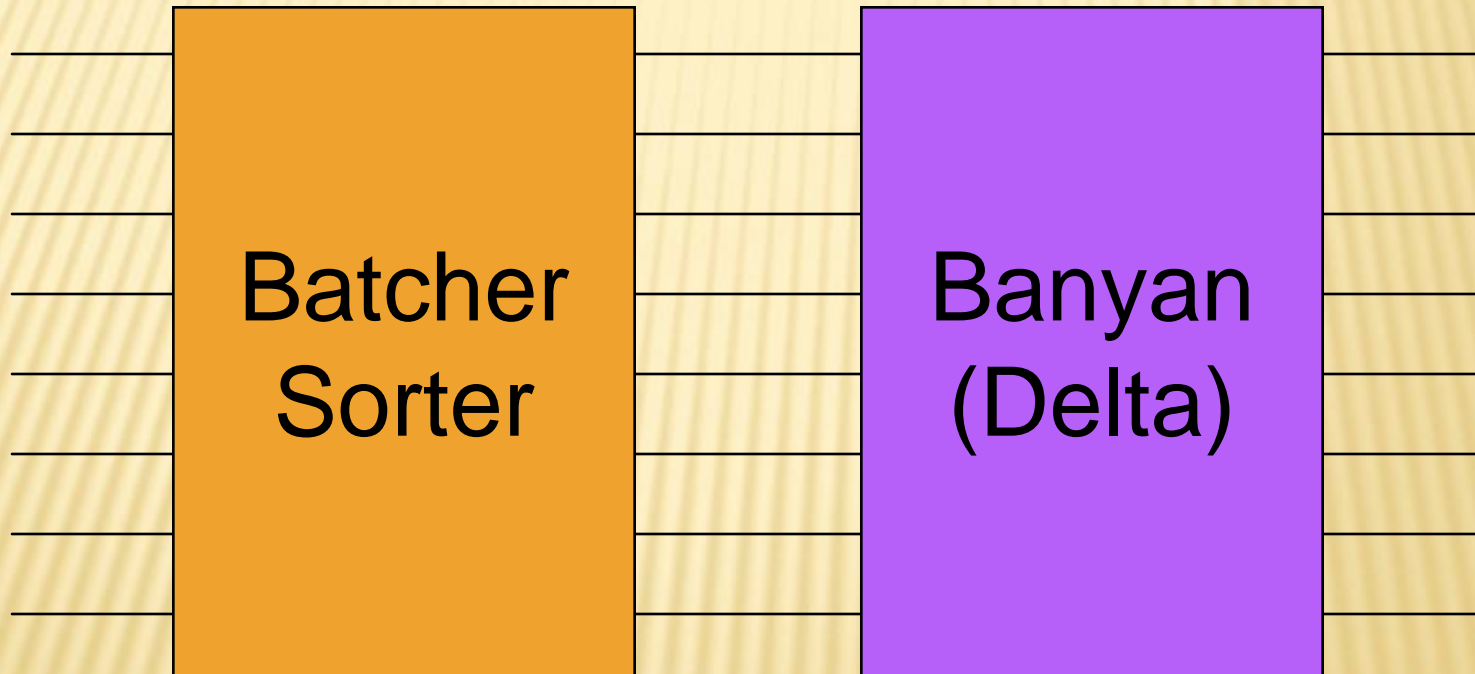
PERFORMANCE DEGRADATION



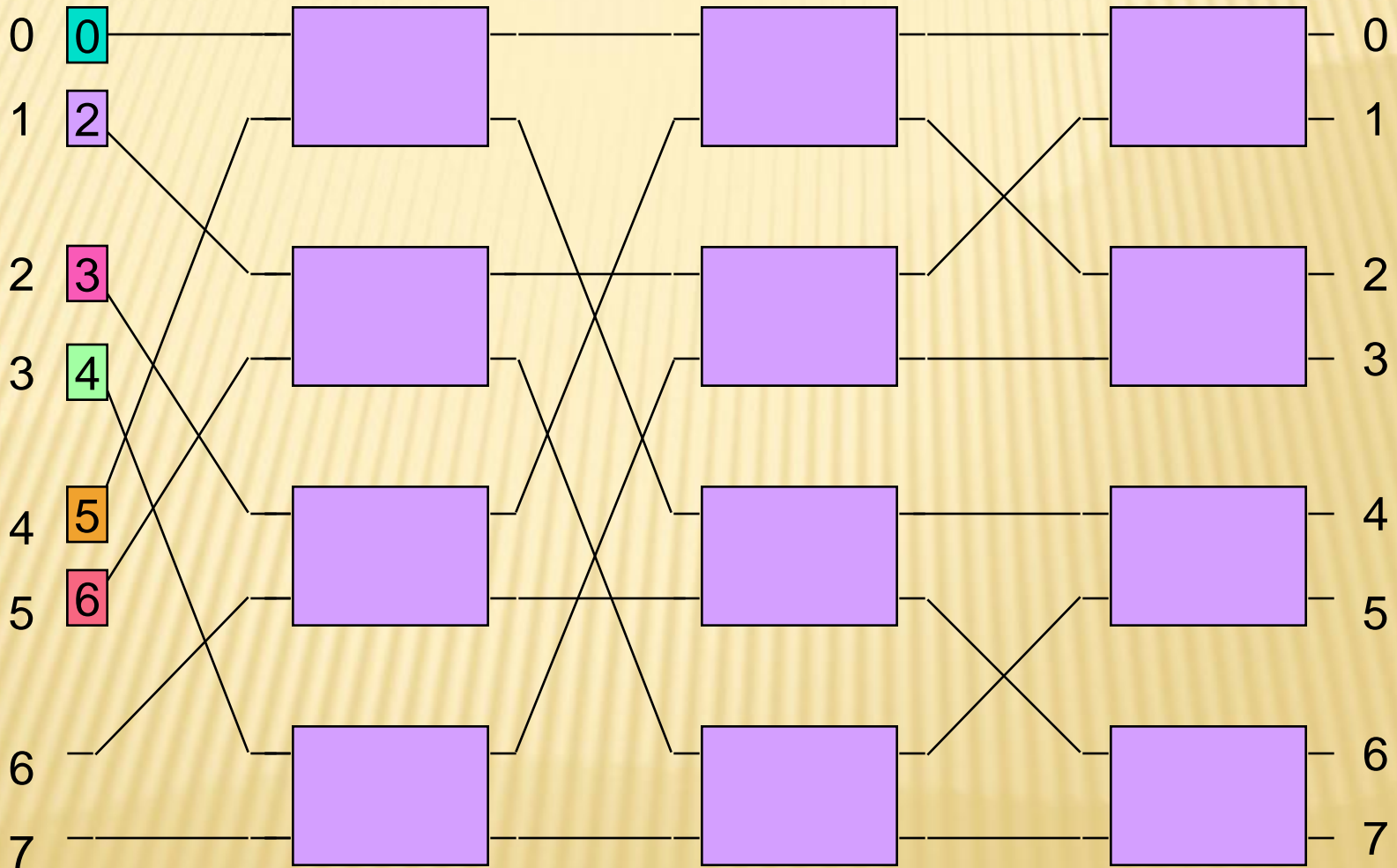
A SOLUTION: BATCHER SORTER

- One solution to the contention problem is to sort the cells into monotonically increasing order based on desired destination port
- Done using a bitonic sorter called a Batcher
- Places the M cells into gap-free increasing sequence on the first M input ports
- Eliminates duplicate destinations

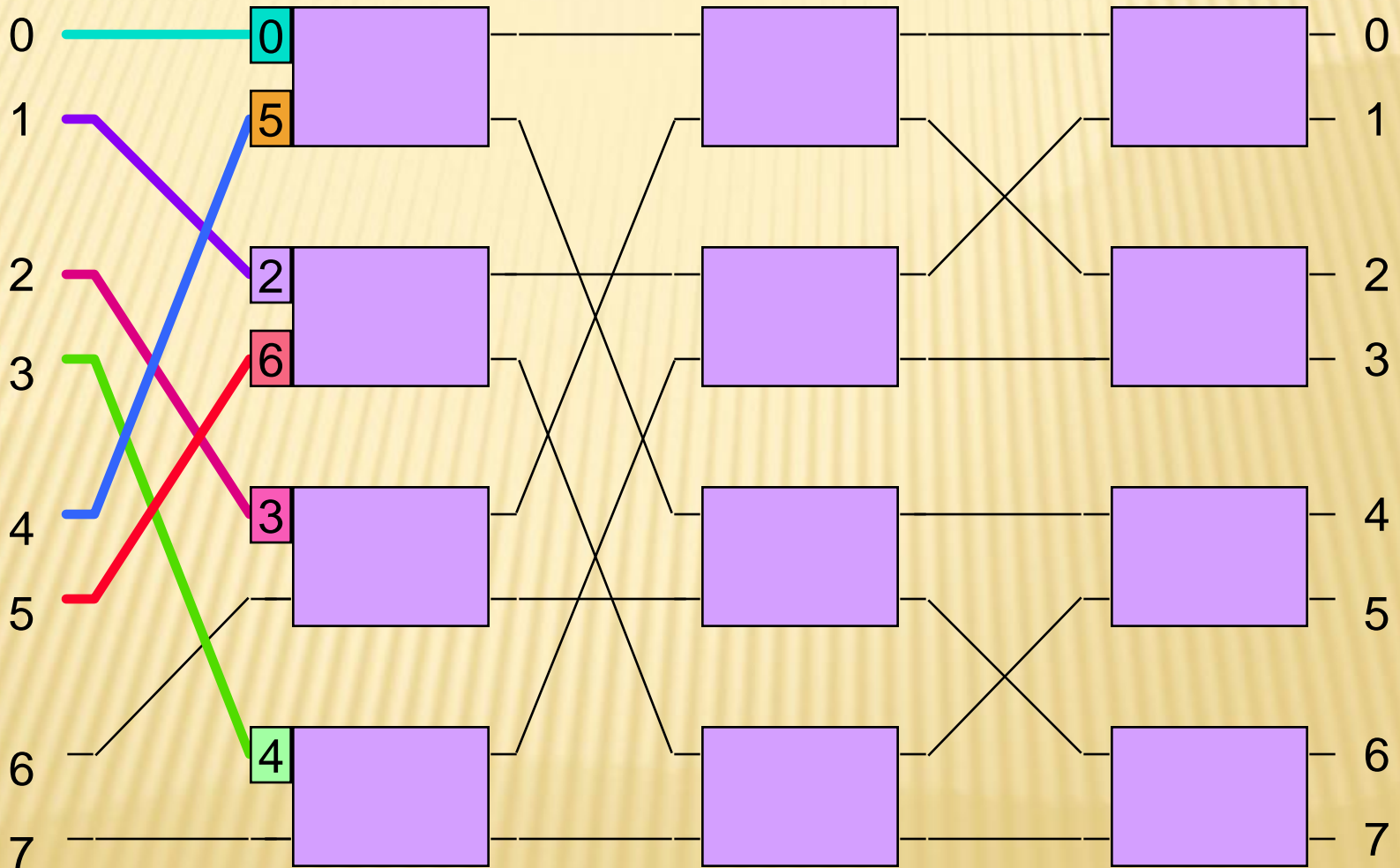
BATCHER-BANYAN



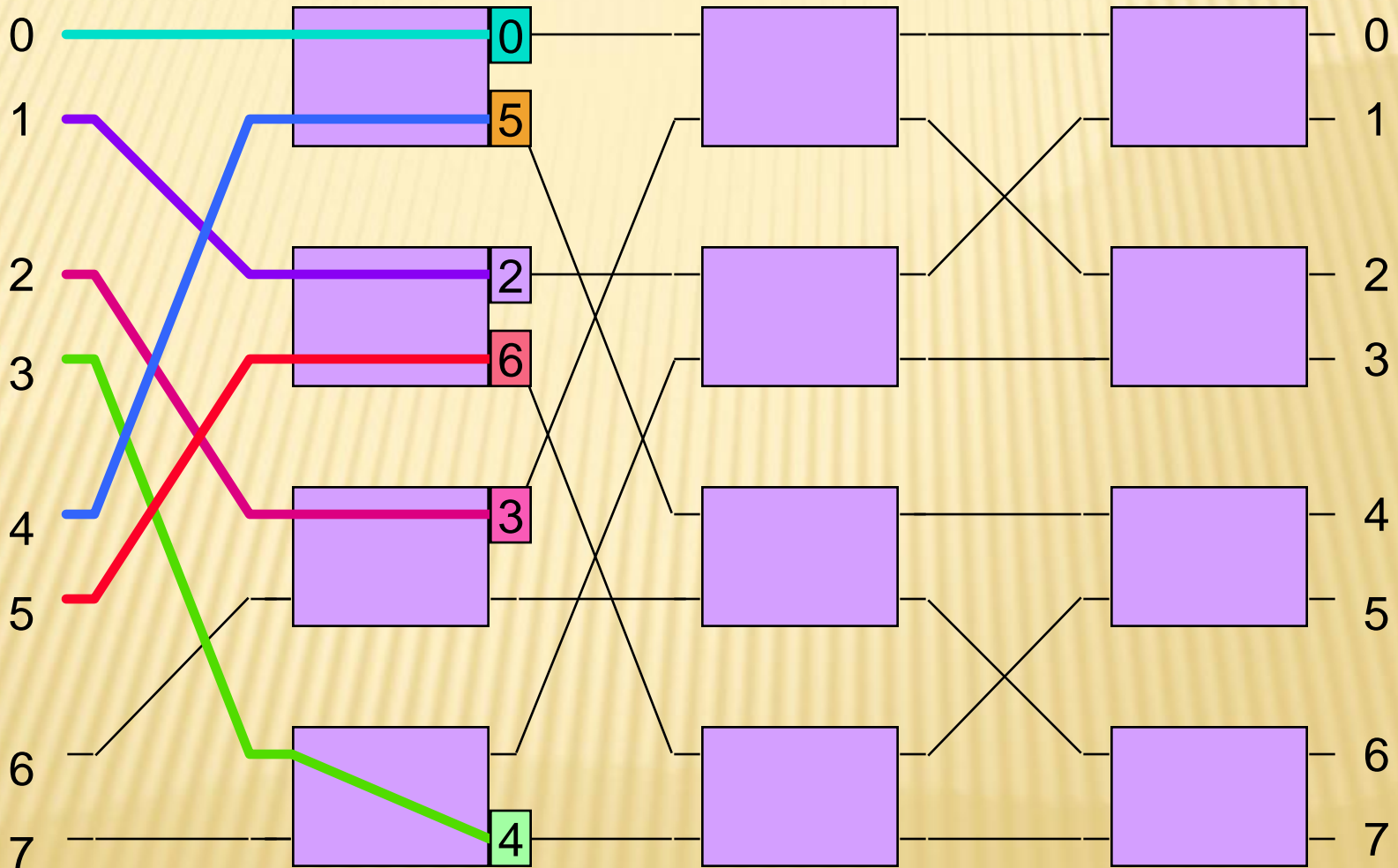
BATCHER-BANYAN EXAMPLE



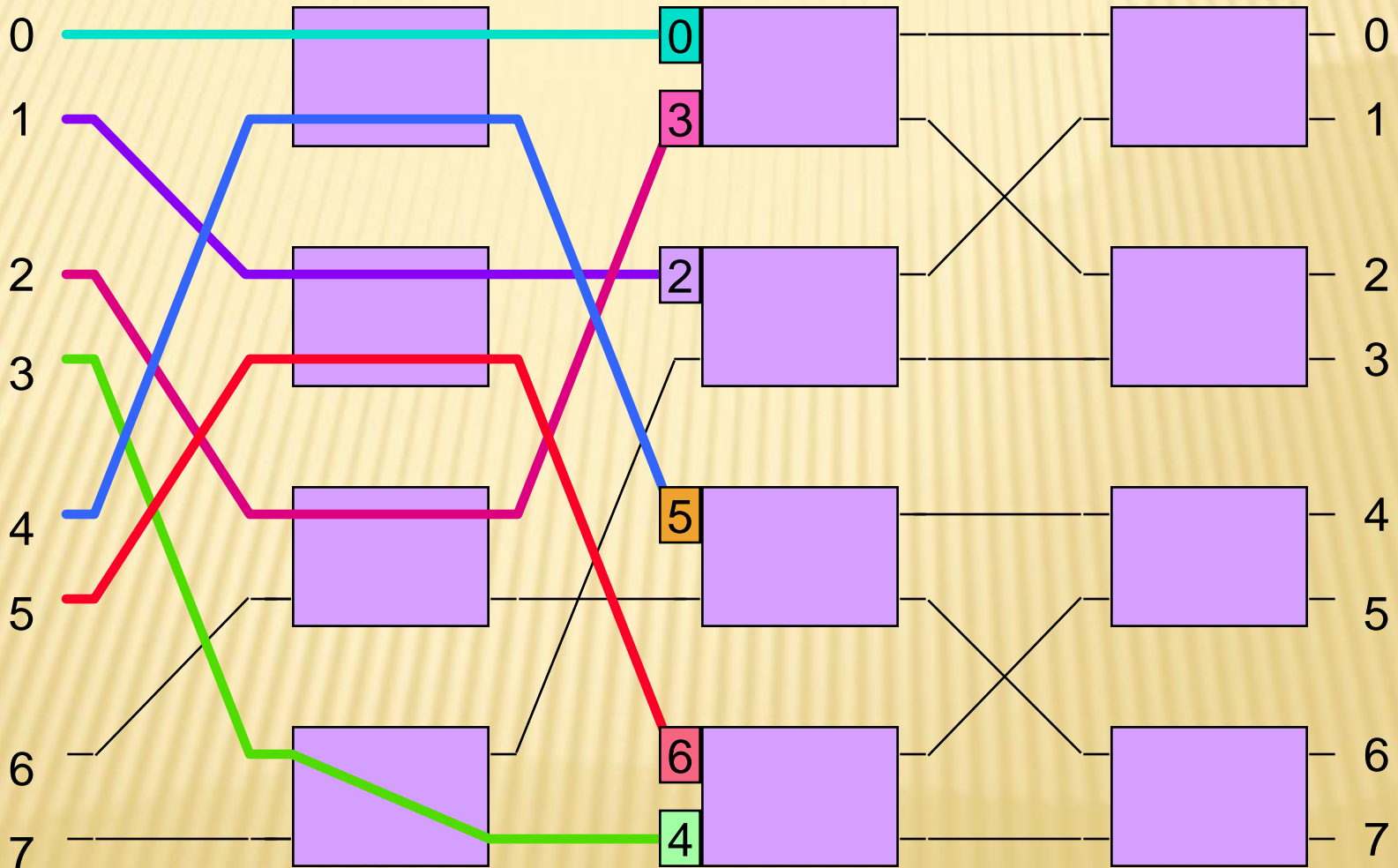
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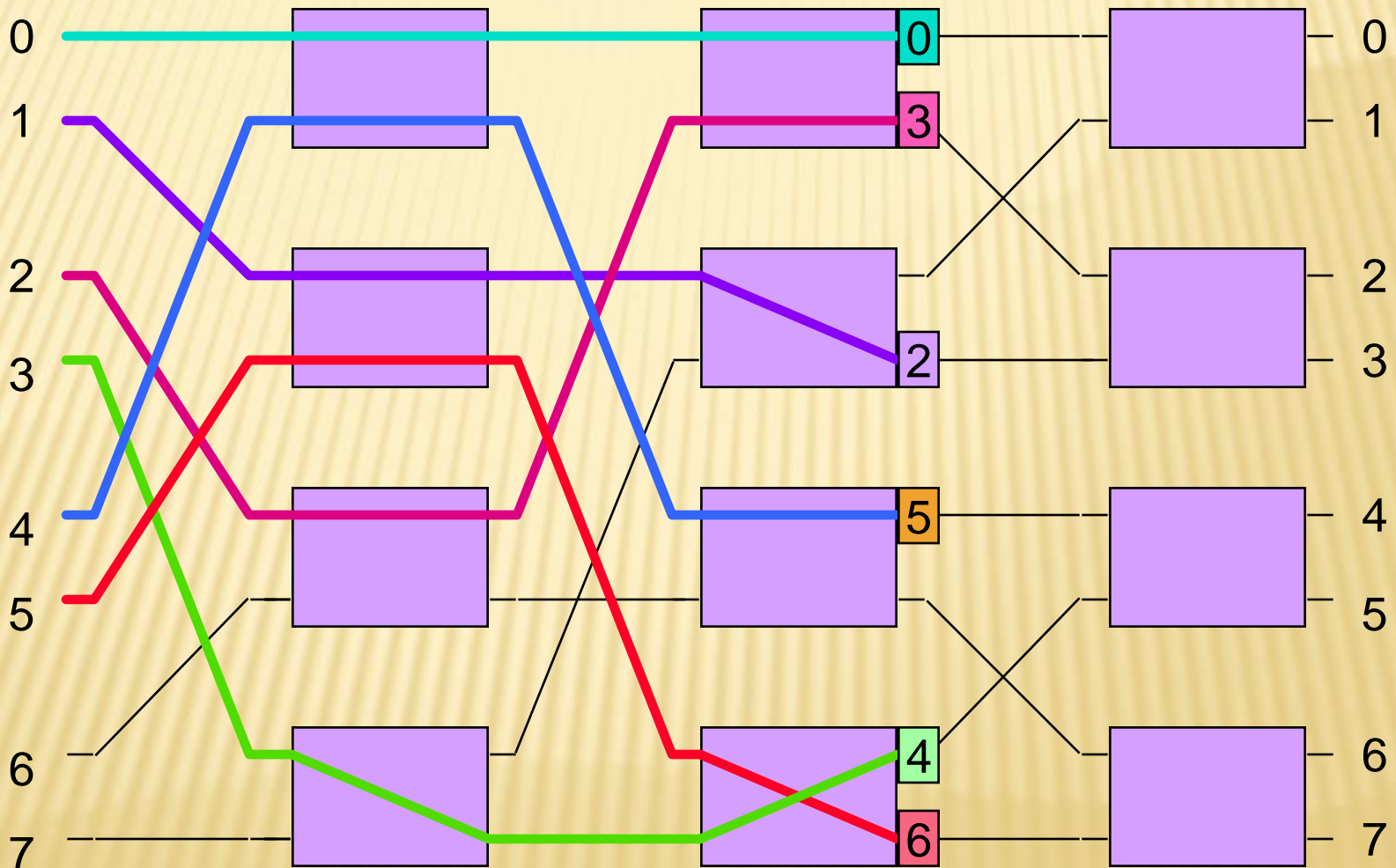
BATCHER-BANYAN EXAMPLE



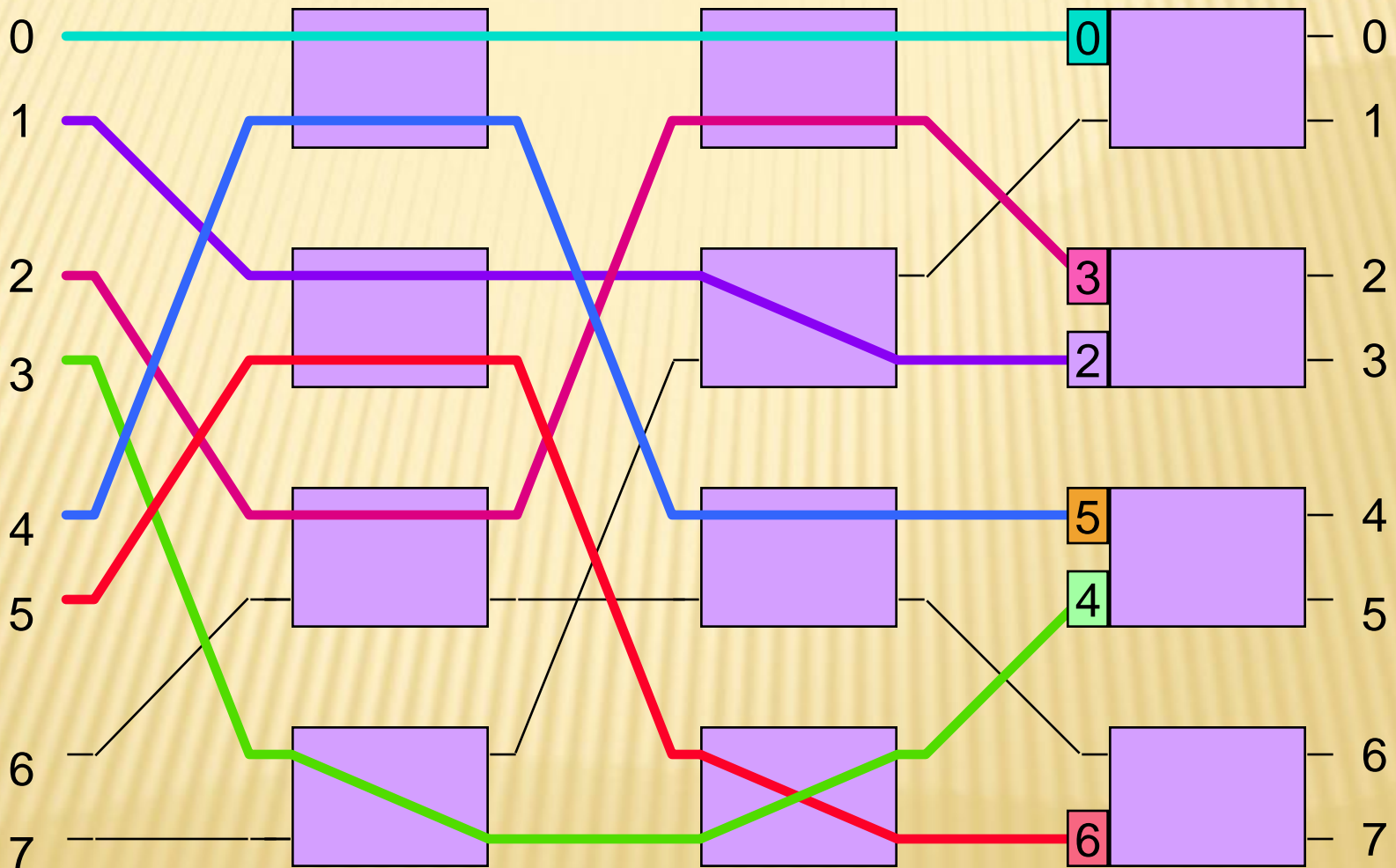
BATCHER-BANYAN EXAMPLE



BATCHER-BANYAN EXAMPLE



BATCHER-BANYAN EXAMPLE



BATCHER-BANYAN EXAMPLE

