

Simulation technique for noise and timing jitter in phase locked loop

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Abstract—: *Timing jitter is a concern in high frequency timing circuits. Its presence can degrade system performance in many high-speed applications. In this paper, a new method for efficiently timing jitter due to phase locked loops is described. Two important parameters, absolute jitter and cycle-to-cycle jitter, used to describe jitter performance can be analyzed. Simulation results for the measurement of jitter in phase locked loop using MATLAB SIMULINK are presented. The methodology described is also applicable to other types of clock generator and oscillators such as LC oscillators, as well as other kinds of noise source such as power supplies.*

Index Terms - key words — *Jitter, oscillator noise, oscillator stability, phase jitter, phase locked loops, phase noise, voltage controlled oscillators.*

1: Introduction

Applications which use phase locked loops (PLLs) for clock and data recovery include optical communication systems, disk drive systems, and local area networks [4]. Other systems including radio transmitters and receivers use phase-locked-loops for frequency synthesis [5], while in complex digital systems such as microprocessors, network routers, digital signal processors and video signal sampling [6,7,8], the clocks used at various points in the system are often synchronized through a phase-locked or delay-locked loop to minimize clock skew [9,10]. Most

of the above systems suffer from jitter, defined in the time domain as random variations in the sampling phase of a signal, or in the frequency domain as phase noise. This is often due to thermal noise and flicker (1/f) noise in the active and passive devices, which make up the components of the PLL system [11], particularly the voltage-controlled-oscillator (VCO). In addition, sudden changes in the supply or substrate can also cause frequency offsets and phase drift. These sources of noise can often be minimized through advanced circuit techniques.

The example shown in Fig.1 for clock signals shows jitter as the short-term displacement of significant events of a digital signal from their ideal positions in time. The expected edges in a digital data stream never occur exactly where desired. Defining and measuring the timing accuracy of those edges (jitter) is critical to the performance of synchronous communication systems.

Jitter is caused by different factors [3]:

- a) Power supply noise passing through a Phase Locked Loop (PLL).
- b) Noise on a PLL's reference frequency signal. A PLL in a frequency synthesizer has a dead-band during which the phase and frequency detector does not detect small changes in the input phase. Since these changes are not detected and corrected, they appear on the outputs in the form of jitter.

- c) Random thermal noise from the crystal reference, or any other resonating device.
- d) Random mechanical noise from vibrations of the crystal reference.
- e) Optical and electrical connectors and cables.
- f) Internal switching noise.
- g) Cross-talk arising from magnetic fields generated by nearby signals produces phase variations in the transmitted digital signal.

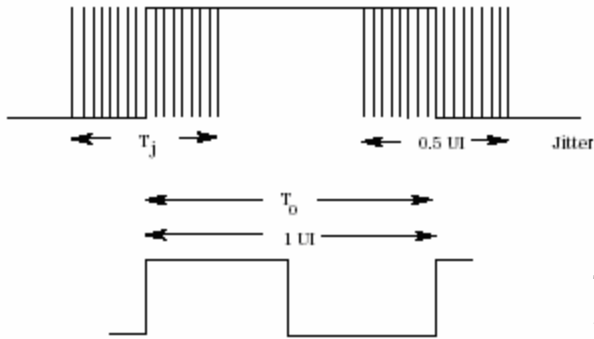


Fig.1: Jitter in clock signals

2.1 Jitter reduction techniques

Different techniques have been reported for the design and implementation of de-jitter circuits or low jitter clock recovery circuits. These techniques include:

- a) The use of additional PLL circuit with Voltage Controlled Crystal Oscillator (VCXO) to get very narrow loop bandwidth.
- b) Modifying the filter design to minimise the phase noise at the VCO input.
- c) Reducing power supply noise.
- d) Eliminating ground bounce.
- e) Using all digital filters with Voltage Controlled Crystal Oscillator (VCXO).

The most commonly used method for controlling jitter in clock recovery circuits is the use of a PLL circuit with narrow filter or VCXO. In this work the effects of using both methods have been studied by simulation using MATLAB SIMULINK. The procedure uses a sinusoidal signal with added random noise that may produce jitter when applied to a zero-crossing circuit with defined saturation levels, where the jitter of the output signal will depend on the added noise

power. The jitter level can be measured using the block diagram shown in Fig. 2. The same arrangement may also be used to compare the jitter levels at different points of a given clock recovery circuit as will be described in the next section.

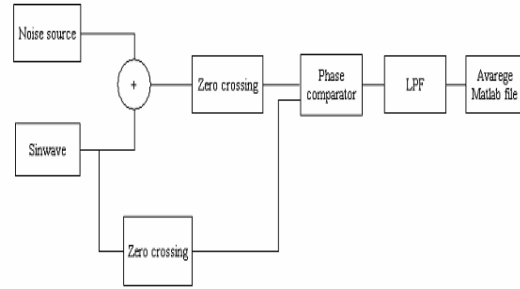


Fig.2 Setup for jitter measurements of noisy signals

The simulation results for Fig. 2 are plotted in Fig. 3 for different power noise levels where we can notice that the output jitter is increased as we increase the added noise. It is to be noted here that the output from the average MATLAB file is in mV and is directly proportional to the jitter level.

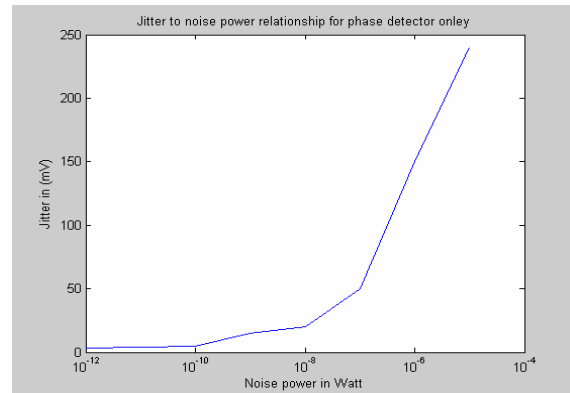
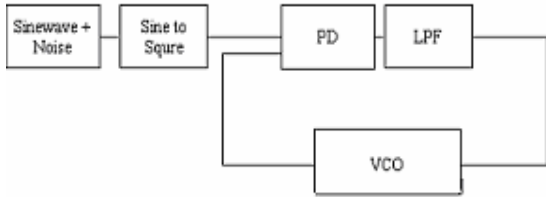


Fig.3: Jitter noise relationship at 10MHz

2.2 Jitter reduction-using PLL

The block diagram of fig.4 shows the PLL used to reduce the jitter associated with a recovered clock signal. Through the simulation we can change the loop bandwidth [1,2] either by changing the loop filter cutoff frequency or by changing the VCO sensitivity. Simulation results are given below.



Phase Locked Loop

Fig. 4: Setup for jitter reduction using PLL

3-Simulation results

Case 1: using narrow band Loop Filter Cutoff frequency:

Referring to Fig.4, which gives the block diagram for the jitter reductions circuit using narrow band PLL. The simulation parameters were chosen as follows:

- $f_o = 10 \text{ MHz}$
- VCO sensitivity = 100 kHz/V
- Loop Filter Cutoff frequency $f_c = 10 \text{ kHz}$
- $V_{in} = 10\sin\omega t$

Square threshold = 1.5V

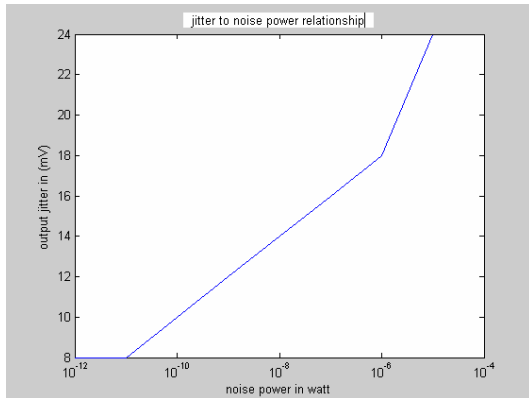


Fig.5: Jitter noise relationship at 10MHz , $f_c = 10 \text{ kHz}$ for PLL loop filter
VCO sensitivity = 100 kHz/V

Using the same procedure defined above, the jitter of the output signals with reference to the same signal (un-noisy signal) are plotted in Fig. 5 where we notice that the PLL can reject the jitter with high efficiency as the noise level becomes appreciable with respect to the signal level while the jitter due to the PLL is relatively clear at very low noise power.

The above simulation is repeated keeping the same parameter while changing f_c to 5 kHz. Fig.6 shows the simulation results for $f_c = 5 \text{ kHz}$. From

the results one can notice that decreasing f_c can reduce the output jitter: at 10^{-6} W noise power jitter level = 13mV instead of 18 mV when f_c was 10 kHz.

Narrowing the PLL bandwidth by using a loop filter of small cutoff frequency may affect its dynamic performance especially the pull in range and pull in time [1,2].

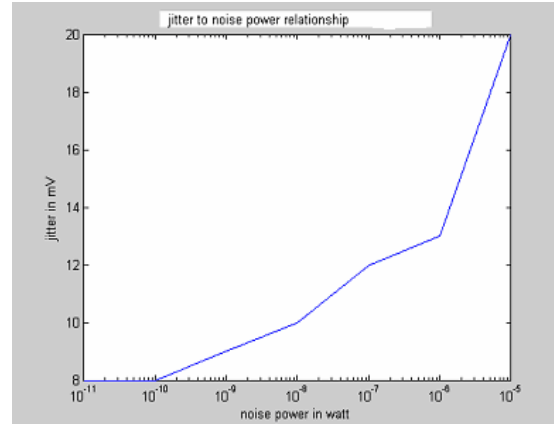


Fig.6 jitter to noise power relationship at 10MHz , $f_c = 5 \text{ kHz}$ for PLL loop filter
VCO sensitivity = 100 kHz/V

Another method that may also narrow the loop bandwidth is to use VCXO instead of using the ordinary VCO circuit. This oscillator has a very narrow band of variation around its center frequency [12].

Case 2: using narrow band VCO (voltage controlled oscillator):

In order to simulate the VCXO we can use the VCO block in MATLAB but with very low sensitivity (in order of several hundreds of Hz around the center frequency).

Referring to Fig.4 and using narrow band PLL, the simulation parameters were chosen as follows:

- $f_o = 10 \text{ MHz}$
- VCO sensitivity = 1 kHz/V
- Loop Filter Cutoff frequency $f_c = 10 \text{ kHz}$
- Square threshold = 1.5V

It is clear from Fig.7 which gives the simulation results when using narrow band VCO that the jitter is also reduced to about but with a little slight amount with respect to Fig. 5 . Available VCXO has a very low sensitivities (about 150 Hz / V in the range of tens MHz). So in practical case we expect more jitter reduction.

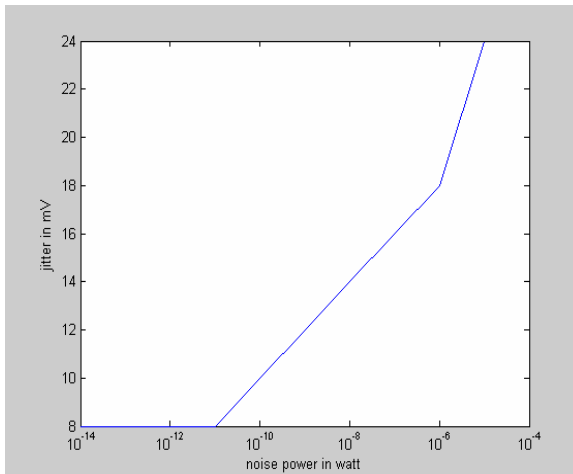


Fig.7 Jitter to noise power relationship at 10MHz, $f_c = 10$ kHz for PLL loop filter VCO sensitivity = 1 kHz/V

4-Conclusion

In this paper a simulation of the jitter measurement setup was carried up using MATLAB SIMULINK software package. It was found that the RMS jitter is increased as the noise power increased, with higher slope above 10^{-6} μ w noise power.

The introduction of the phase locked loop highly reduces the output phase jitter especially when the noise power is high. At low noise levels the PLL itself may keep a constant jitter level due to the voltage-controlled oscillator because the output of the low pass filter flickers.

In the setup the jittered and un-jittered (reference) signals are applied to the input of the phase detector (PD). The output of the phase detector is the input of low-pass filter, which feeds the M-file of the SIMULINK. The contents of the M-file are processed to get the RMS jitter. The simulation results show the validity of using a PLL with either narrow loop filter or narrow band VCO to reduce jitter.

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