

## ABSTRACT

Timers are widely used in so many applications. Among such applications we mention the most **Popular applications**: heaters, filters, pumps, fans, signs, blowers, indoor and outdoor lighting, feeders, security/alarm systems, watering systems, and process controls. Modern timers make use of the great development in digital electronics, and acquire so many features rather than absolute timing operations. Examples of such features are:

- **High timing precision extending from  $\mu$  seconds to several hours.**
- **Full programmability along day, week and even month.**
- **Possibility of repeat programs provide up to several switching cycles per week.**
- **Low weight and low power consumption.**
- **Battery operation provides outdoor function.**
- **Simple and fast setting by means of push buttons and display prompts.**

The price of such timers is ranging from 50 US\$ up to several hundreds US\$ according to their features and power capabilities. On the other hand, the circuit design, testing and implementation of such equipments using local experience is possible and can be carried out.

The main objective of this project is to develop a low cost timer module that may be fabricated locally, and meets the most features available in the international market. The basic concept in realizing this objective is to make use of the Series Switched Capacitor (SSC) technique introduced in 1993 as the basic timing element in the timer circuit [1]. This technique enables wide time programming range using the same capacitor. The

limitation of employing the SSC in producing commercial timers before was due to the relatively large area needed for building the control circuit [2]. The control circuit was completely built using available standard SSI and MSI circuits. Throughout this project the overall control circuit in addition to the other added features like display , control data entry ...etc will be implemented on a single VLSI chip using FPGA ( Field Programmable Gate Array) or other programmable technology, such as low cost microcontrollers, according to the cost and the available tools. This new technologies becomes today the best solution for implementing digital system on single chip without going through the complex process of developing a special purpose IC. Digital design using programmable Logic devices (PLD) or microcontrollers is a cost effective way to save time, cost and get high system performance as regarding added features, power consumption, sizing and reliability.

## ملخص

تعتبر أجهزة التوقيت من الوحدات الرئيسية في الأنظمة الصناعية كما أن لها استخدامات عديدة في حياة الإنسان اليومية و نذكر منها: أنظمة الإضاءة بالمنازل و الشوارع، أنظمة الإنذار ضد السرقات و الحريق، أنظمة الري. الخ.. ولقد استفادت أجهزة التوقيت الحديثة من تكنولوجيات الالكترونيات الرقمية لتحسين دقة التوقيت وإضافة مزايا عديدة أخرى مثل إمكانية البرمجة المسبقة على مدى اليوم و الأسبوع والشهر. و تعد هذه المزايا مع رخص السعر و قلة استهلاك القدرة الكهربائية من المواصفات الهامة عند اختيار و شراء أجهزة التوقيت. وتتراوح أسعار أجهزة التوقيت من حوالي خمسون دولار أمريكي إلى عدة مئات الدولارات وذلك طبقا لمزاياها و قدراتها الكهربائية. و الجدير بالذكر انه لا يوجد منتج محلي من أجهزة التوقيت على الرغم من سهولة تصميمها و تصنيعها بالإمكانات و الخبرة المحلية.

و الهدف الرئيسي من هذا المشروع البحثي هو تطوير جهاز توقيت ذو مزايا إضافية محلية بحيث يمكن تصنيعه وتسويقه داخل المملكة بأسعار أقل بكثير من سعر مثيله المستورد بخبرة من الخارج. والمبدأ الأساسي لبناء الدائرة الإلكترونية الخاصة بجهاز التوقيت المقترح تعتمد على استخدام المكثف التبادلي المتوالي كعنصر توقيت قابل للبرمجة و يعطى قيمة متغيرة على نطاق واسع جدا. و قد طرحت هذه الفكرة لأول مرة عام 1993 ولكن كان هناك صعوبة في تنفيذها نظرا للمساحة الكبيرة التي كانت تلزم لبناء دائرة التحكم مما يجعل الجهاز غير منافس إذا أخذنا الحجم و استهلاك القدرة الكهربائية في الاعتبار. ومع استحداث تكنولوجيات مصفوفات البوابات المنطقية المبرمجة FPGA والحاسبات الدقيقة المدمجة أمكن إعادة التفكير في إمكانية التصميم مرة أخرى و تحقيق الأهداف المذكورة سابقا. وتعد هذه التكنولوجيات من الأساليب التي يمكن استخدامها في الدول النامية لبدأ صناعات إلكترونية محلية يمكن أن تنافس المستورد من حيث الأداء و السعر.

# **CHAPTER I**

## **TIMER CIRCUITS**

### **I-1 INTRODUCTION**

Time measurements or time control are still up today one of the most challenges that man faced since he started his industrial revolution. The transfer from mechanical timing systems to electronically controlled system is considered a real step in both time measurements and control.

Today digital clocks and digitally controlled timers are found any where and every where in our daily life. Most of our home appliances are equipped with electronic timers , examples are washing machines , microwave furnaces , telephone and TV sets ...etc. other application may be found in industry such as in process control , medical and chemical process , irrigation systems, lighting systems and photocopying machines .Actually one can not count all timer application as they are spread and needed in all applications in our modern life.

Basically electronic timers modules are built around an Integrated Circuit where an external capacitor and resistor elements are added to operate the circuit and determine the time interval. Additional digital circuits may be added to make the timer digitally programmable using external switches or keyboards. Since the year 1971 when the 555 timer IC was first introduced it became one of the important building blocks in automated system as it represents the heart of any industrial or commercial timer module. It provides the circuit designers and hobbieist with a relatively cheap, stable,

and user-friendly integrated circuit for both monostable and astable applications. This timer after more than 30 years is still very popular and used in many schematics. The objectives of many research during the last 20 years were to design a fully programmable timer modules that cover different requirements of users . Among these requirements we mention:

- 1- Programmability using easy digital method.
- 2- Provide wide range of time intervals from very short times ( ms ) up to long time periods ( several hours ) with high precisions .
- 3- Low cost and high reliability.
- 4- Provide high resolution in time selection.

The main objective of this research is to develop a timer module that covers the above requirements.

The proposed module will use the well known 555 timer IC chip in its normal monostable mode of operation. A digitally controlled series switched capacitor (SSC) technique will be added to achieve the above mentioned requirements. In the next section the theory of SSC is introduced and explained.

## **I-2 The Series Switched Capacitor**

Consider a capacitor in series with a Voltage Controlled Switch (VCS) as shown in Fig.1.1a while the control switching signal is a train of pulses as shown in Fig.1 b. The state of charging this capacitor will depend on the duty cycle of the switching signal. One approach to find the relation between the equivalent capacitance when connected in series with a VCS and the switching duty cycle is to perform a time charge analysis. The VCS is only ON during  $\tau$  seconds each period  $T$  of the switching signal. If we

assume that the total ON time of the VCS needed by the capacitor is to reach a certain voltage  $V_c$  is  $T_1$  then we may write:

$$T_1 = N\tau = N d T \quad (1.1)$$

Where  $d$  is the duty cycle of the switching pulsed

$$D = \tau/T \quad (1.2)$$

$N$  is the number of periods counted during the charging process through which the capacitor voltage is increased from zero to  $V_c$ . The real time elapsed is then:

$$T_{\text{real}} = NT \quad (1.3)$$

Substituting equations (1.1) , (1.2) in equation (1.3) gives

$$T_{\text{real}} = NT = T_1/d \quad (1.4)$$

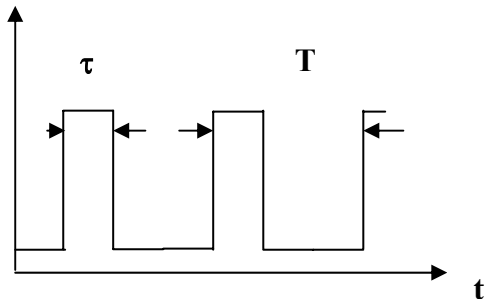


Fig. 1.1b Switching signal

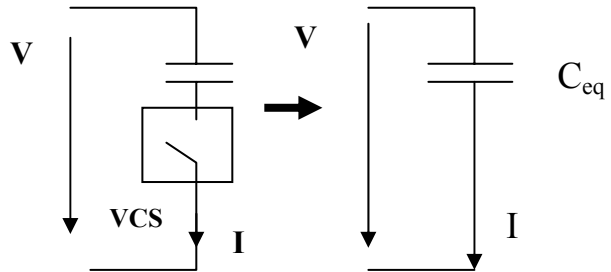


Fig. 1.1a Series switched capacitor

Now consider another capacitor  $C_{eq}$  whose value is chosen such that it takes time equal to  $T_{real}$  to be charged from zero volts to  $V_c$  from the same source, and since the same charges will be delivered for both capacitors then we may write:

$$C_{eq} T_1 = C T_{real} \quad (1.5)$$

$$C_{eq} = C/d \quad (1.6)$$

Equation (1.6) shows that the effective capacitor value will be increased since  $d$  is often less than 1.

The SSC has so many applications in different domains such as communications, instrumentation, time and frequency control ...etc. It is already used to implement all types of filters, phase shifters, sinusoidal oscillators and timing circuits[1-4]. The importance of such technique is due to the possibility of implementing a capacitor with large values, high precisions, low cost, and full programmable. These features help in building many circuits and application in the above mentioned domains.

It is to be noted here that a frequency domain analysis can also be performed to obtain the equivalent value of the SSC. This analysis is given in details in ref [5] and leads us to the same result given by equation (1.6).

### **I-3 THE 555 IC TIMER**

The internal circuit of the 555 timer is given in fig.1.2 [5]. All IC timers rely upon an external capacitor to determine the off-on time intervals of the output pulses. As it takes a finite period of time for a capacitor ( $C$ ) to charge or discharge through a resistor ( $R$ ),

those times are clearly defined and can be calculated given the values of resistance and capacitance.

### I-3.1 Operating Modes of the 555 timer

The 555 timer has two basic operational modes: one shot and astable. In the one-shot mode, the 555 acts like a monostable multivibrator. A monostable is said to have a single stable state--that is the off state. Whenever it is triggered by an input pulse, the monostable switches to its temporary state. It remains in that state for a period of time determined by an RC network. It then returns to its stable state. In other words, the

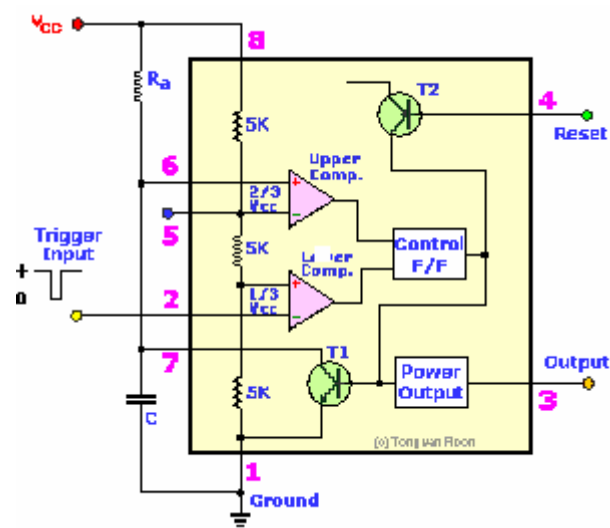


Fig. 1.2 555 Timer block diagram

monostable circuit generates a single pulse of fixed time duration each time it receives an input trigger pulse, thus the name one-shot. One-shot multivibrators are used for turning some circuit or external component **on** or **off** for a specific length of time. This is shown in Fig.1.3

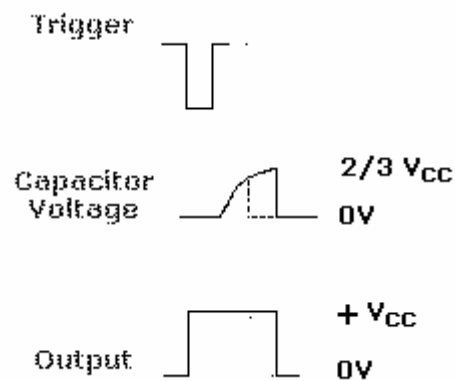


Fig. 1.3 Monostable waveforms

The circuit is sensitive to input pulse frequency and reset input. If it receives a reset signal the output pulse will go down. On the other hand additional triggering pulse has no effect if it is active before the capacitor voltage reaches  $2/3 V_{CC}$

The other basic operational mode of the 555 is as astable multivibrator. An astable multivibrator is simply an oscillator.

The astable multivibrator generates a continuous stream of rectangular off-on pulses that switch between two voltage levels. The frequency of the pulses and their duty cycle are dependent upon the RC. The basic waveform associated with astable operation is shown in Fig.1.4.

#### **I-4 MONOSTABLE CIRCUIT**

Fig.1.5 shows the basic circuit of the 555 connected as a monostable multivibrator. An external RC network is connected between the supply voltage and ground.

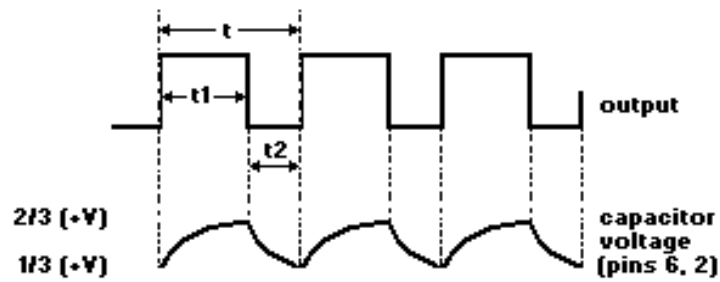


Fig. 1.4 Astable waveform

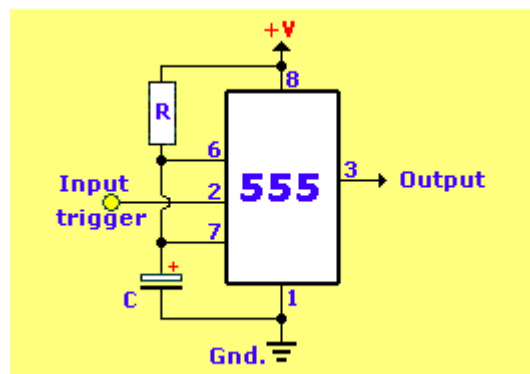


Fig.1.5 Monostable circuit

The trigger input is initially high (about  $1/3$  of  $+V$ ). When a negative-going trigger pulse is applied to the trigger input, the threshold on the lower comparator is exceeded. The lower comparator, therefore, sets the flip-flop. That causes transistor T1 to cut off, acting as an open circuit. The setting of the flip-flop also causes a positive-going output level which is the beginning of the output timing pulse.

The capacitor now begins to charge through the external resistor. As soon as the charge on the capacitor equal  $2/3$  of the supply voltage, the upper comparator triggers and

resets the control flip-flop, that terminates the output pulse which switches back to zero. At this time, T1 again conducts thereby discharging the capacitor. If a negative-going pulse is applied to the reset input while the output pulse is high, it will be terminated immediately as that pulse will reset the flip-flop.

Whenever a trigger pulse is applied to the input, the 555 will generate its single-duration output pulse. Depending upon the values of external resistance and capacitance used, the output timing pulse may be adjusted from approximately one millisecond to as high as on hundred seconds. For time intervals less than approximately 1-millisecond, it is recommended that standard logic one-shots designed for narrow pulses are used instead of a 555 timer. IC timers are normally used where long output pulses are required. In this application, the duration of the output pulse in seconds is approximately equal to:

$$T_o = 1.1 \times R \times C \text{ (in seconds)} \quad (1.7)$$

### **I -5 ASTABLE CIRCUIT**

Fig. 1.6 shows the 555 connected as an astable multivibrator. Both the trigger and threshold inputs (pins 2 and 6) to the two comparators are connected together and to the external capacitor. The capacitor charges toward the supply voltage through the two resistors, R1 and R2. The discharge pin (7) connected to the internal transistor is connected to the junction of those two resistors.

The frequency of operation of the astable circuit is dependent upon the values of R1, R2, and C. The frequency can be calculated with the formula:

$$f_o = 1/ (.693 \times C \times (R1 + 2 \times R2)) \quad (1.8)$$

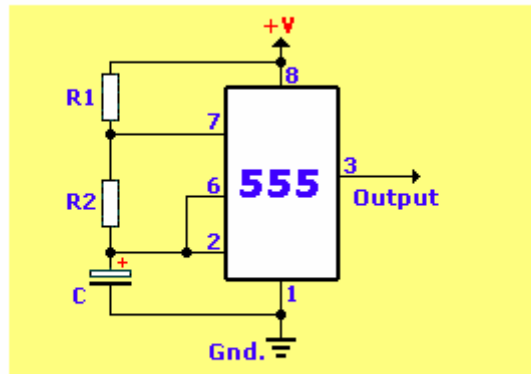


Fig. 1.6 The 555 connected as an astable multivibrator

### I-6 COUNTER /TIMER ICS

Several IC chip timer are available from several manufacturers [6]-[15]. They are similar in operation with the 555 timer introduced above. The comparison of electrical specification , performance characteristics , basic features, package types and original and other manufacturers of the commercially available timer ICs are presented in table 1-1 [16]. The timer circuits given in table 1-1 are of the single cycle type with maximum time delay of about 18 minuets using capacitors in excess of 100  $\mu\text{F}$  and a resistor as large as 10 M  $\Omega$  [17].At this maximum limit , precision are difficult to obtain and when available they tend to be very expensive . In addition, the leakage currents of the internal discharge transistor and the base current of the comparators become comparable to the charge and discharge currents of the capacitor. An alternative to overcome the problem of achieving long time delays is to use timer / counter –type circuits. They contain a precision time- base oscillator that derives a built- in counter stage. This counter may be either fixed or programmable according to the application.

Table 1-1 Comparison of one shot timers

Several IC chip timer/ counter ICs are available from several manufacturers [18]-[26]. The comparison of electrical specification, performance characteristics, basic features, package types and original and other manufacturers of the commercially available timer ICs are presented in table 1-2 [27]. **In the next section a completely different approach for realizing programmability and extra long delay timer circuits is presented and analyzed.**

### **I-7 Timer circuit with SSC**

A timer circuit with SSC is as same as given by figures 1.4 and 1.5 except that we insert a VCS in series with the timing capacitor. Replacing the capacitors in equations (1.7) and (1.8) by the equivalent value given by equation (1.6) will result:

For the Monostable circuit:

$$T_o = 1.1 \times R \times C/d \quad (1.9)$$

And for the Astable circuit:

$$f_o = 1/d (.693 \times C \times (R1 + 2 \times R2)) \quad (1.10)$$

Equations (1.9) and (1.10) show the possibility of controlling both time and frequency by varying the switching duty cycle d. A complete digitally programmable timer circuit may be realized if d is to be digitally controlled. This is the major objective of this project and the details will be given later.

### **I-8 EXPERIMENTAL VERIFICATIONS**

To verify and study the behavior of the timer circuits with SSC, the 555 timer is wired in both Monostable and astable modes of operation. As expected the charging

/discharging curve of the timing capacitor is in form of ascending and descending staircase wave form. As shown in figures 1.7 and 1.8 the capacitor stops charging during the off period of the switch while it follows its charging curve during the ON period. Equation (1.9) is also verified by plotting the output pulse duration  $\tau$  versus the duty cycle  $d$  as given by Fig.1.9. Fig.1.10 represents the relation between the output frequency in kHz and the switching pulse duty cycle where we notice the exact compatibility between measured and calculated results. These two experimental curves reflect the high precision of such technique and ensure its efficiency and reliability for implementing accurate and precise timer modules for industrial and commercial applications.

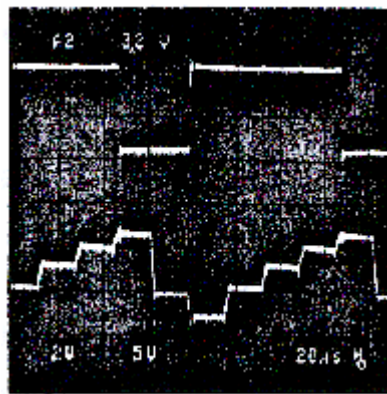


Fig. 1. 7 Upper : Monostable output  
Lower : Capacitor voltage

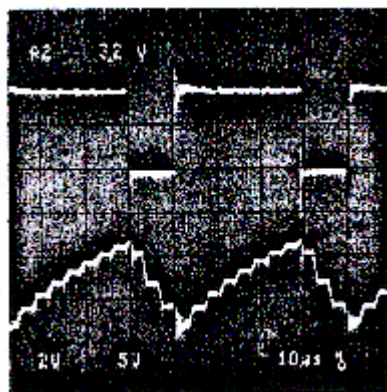


Fig 1.8 Upper : Astable output  
Lower : Capacitor voltage

**Table 1-2 Comparison of Timer/ Counters ICs**

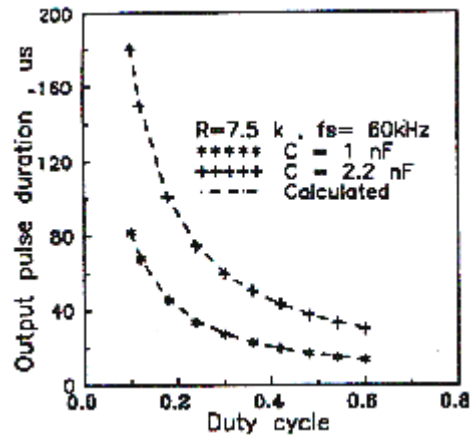


Fig. 1.9 Dependence of  $T_o$  on  $d$

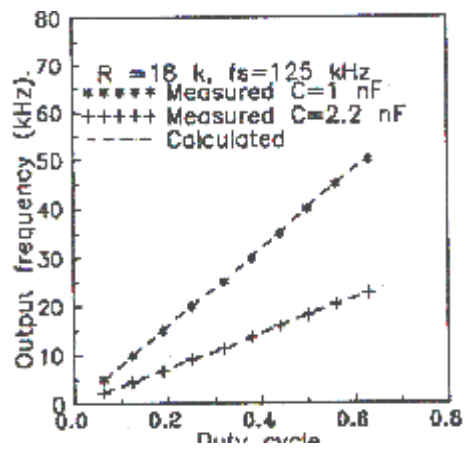


Fig. 1.10 Dependence of  $f_o$  on  $d$

# **CHAPTER II**

## **DIGITALLY CONTROLLED DUTY CYCLE PULSE GENERATOR CIRCUIT (THE DISCRETE VERSION)**

### **II-1 INTRODUCTION**

Several timer modules are available from different manufactures [28-33]. They make use of the great development in digital electronics, and acquire so many features rather than absolute timing operations. Examples of common such features are:

- **High timing precision extending from  $\mu$  m seconds to several hours**
- **Full programmability along day, week and even month.**
- **Possibility of repeat programs provide up to several switching cycles per week.**
- **Low weight and low power consumption.**
- **Battery operation provides outdoor function.**
- **Simple and fast setting by means of push buttons and display prompts.**

The proposed timer module covers most of the above features while employing a new approach for programmability. As shown in chapter I the design of a digitally controlled duty cycle pulse generator circuit is the main objective in this work. The performance and accuracy of this circuit will determine the overall performance of the timer modules especially the time interval accuracy and resolution. Other features of this circuit are its ability to receive external digital commands in an easy way and its small volume and low power consumptions. The basic elements of the implemented timer module are shown in Fig.2.1 where we can identify the following circuits:

1-Time Mode Select Switch (TMSS) : the function of this part is to enable the user to select at first the time mode, we have two modes:

A- H M S, in this mode the required time interval is entered by the user in Hour, Minute, Second format with 10 sec resolution. This means that the accuracy of the timer in this mode is 10 sec.

B- ms, in this mode the required time interval is entered by the user in millisecond format with 10 ms resolution. This means that the accuracy of the timer in this mode is 10m sec.

2- Time entry and control circuit: the function of this circuit is:

A- Setting the time interval in either format.

B- Reset all the timer operation to its initial conditions.

C- Send a trigger input to the timer circuit.

3- Digital data generator circuit: the function of this part is to receive signals from the time entry circuit and process these signals to produce the digital data needed by the duty cycle controller.

4- The Display: This part display the required time interval in either formats described above.

5- The duty cycle controller: This circuit receives digital data and converts them into pulses with variable duty cycle.

6- SSC circuit: a timing capacitor connected in series with a Voltage Controlled Switch. The On- Off control signal of this switch is the output from the duty cycle controller.

7- 555 timer circuit: receives a trigger signal from the Time entry circuit and produces an output pulse with time interval equal to the displayed value. The timing element for this circuit is a simple resistor and a SSC.

8- A power relay 110/ 220V /8A: this relay switch the power ON across the load during the time interval chosen by the user and started by the trigger pulse. Notice that the power level of this relay may be increased and it is independent on all the above circuits.

9- Power Supply Unit: to provide the power needed to operate the above described parts.

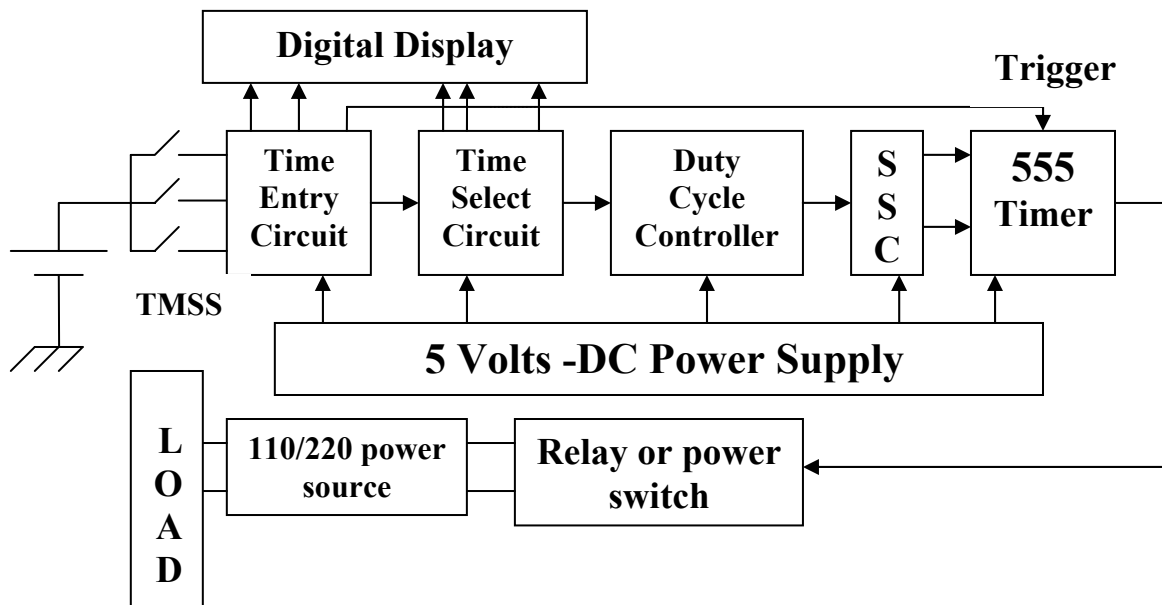


Fig. 2.1 Timer module block diagram

Two approaches for implementing the above block diagram may be used. The first is to use the available off- shelf digital SSI and MSI IC,s . The second is to use a programmable circuit such as an FPGA or microcontroller. Two versions had been designed built and tested at the laboratory, each employs either approach. The purposes of using the first approach were to optimize the design as regarding the system functions like the user interface, the display ...etc, also to get an optimal definition for the logic sequence, signals and data processing. A comparison is also presented between the two approaches as regarding cost, circuit complexity, power consumption and size. Circuit details as well as logic operation will be explained in the following sections. Both versions use the same mathematical model that will be given in the next section.

## **II-2 THE MATHEMATICAL MODEL**

Referring to the system block diagram shown in Fig.2.1 assuming that the On time of the switching pulses used to control the SSC is fixed and equal to  $10 T_x$ .

Where  $T_x$  is the period of the master crystal oscillator deriving all the timing functions of the system.

The frequency of the switching pulses is

$f_s = 1/T_s = 1/10MT_x$  where M is an integer selected by the user to set the required time interval.

The switching duty cycle is then given by :

$$d = 1/M \tag{2.1}$$

The equivalent capacitor is given by

$$C_{eq} = C/d = MC \tag{2.2}$$

The output time interval from the timer:

$$T_o = 1.1 R C_{eq} = M (1.1 RC) \quad (2.3)$$

**Time modes:**

Two modes are proposed and can be selected using external switch :

**Mode 1:** H M S mode where time is selected in Hour/ Minute / second format. In this mode the range for  $T_o$  is  $10 \text{ sec} < T_o < 24 \text{ hours}$  with 10 sec step.

$$1 < M < 8640 \quad (8640 \times 10 \text{ secs} = 24 \text{ Hours})$$

$$1.1 RC = 10 \text{ secs} \quad C = 10 \mu\text{F} \quad R = 908 \text{ k } \Omega$$

We may use 1 M  $\Omega$  pot.

**Mode 2:** ms mode where time is selected in ms format . In this mode the range for  $T_o$  is  $10\text{ms} < T_o < 999.99 \text{ sec}$  with 10 ms step.

$$1 < M < 99999$$

$$1.1 RC = 0.01 \text{ sec} \quad C = 10 \text{ nF} \quad R = 908 \text{ k } \Omega$$

use 1 M  $\Omega$  pot.

## **II-3 SYSTEM DESCRIPTION AND IMPLEMENTATION**

The system given in Fig 2.1 is completely designed, built , and tested to meet the specification described above. The circuit details are given below. Fig. 2.2 gives the circuit details for the following parts:

1- Time entry and control circuit.

2- Digital data generator circuit.

3- The Display.

4- The duty cycle controller.

### **II.3.1 Time entry and control circuit.**

This part contains :

- One 3-bit binary counter C2 SN 4790 MSI IC chip
- One 3 lines to 8 lines decoder SN 74 138 MSI IC chip
- One de-bounced switch S2
- One Master Reset Switch S3

When S3 is pressed all counters are reset to their initial value , the 3 bit counter C2 outputs are then 000. The counter output are the ABC inputs of the decoder circuit whose function is to activate only one of its 8 outputs Y0 to Y7, Y0 is now going low. Pressing S2 once will increment the counter and activate the output Y1. The outputs from Y0 to Y4 are used to control the operation of the digital data generator circuit.

### **II-3.2 Digital data generator circuit.**

This part contains:

- One 4-bit binary counter C1 SN 4790 MSI IC chip

- Five 4-bit Latch CD 4042 MSI IC chip
- One de-bounced switch S1

The counter C1 is incremented each time S1 is pressed, so any binary code from 0000 to 1111 (decimal value from 0 to 15) can be reached. The output 4-bits from C1 are then represent 4-bit data bus (the heavy solid lines in Fig. 2.2) which are common to the data input of the 4-bits latches. As this type of latch circuits becomes transparent when its strobe input goes low, the Y outputs Y0 to Y4 are used as the strobe inputs of the 5 latches. Like this, any of these latches can be addressed individually according to the output of the counter C2. The binary data presented on the data bus will be transferred and displayed on the 7-segment display to give the number in decimal format. The user increment C1 until it reaches the selected predetermined value. At this moment the user stops incrementing C1 and increments C2. When this later is incremented it activities the next output of the decoder circuit (Y – output), allowing the selection of the next digit. Starting from master reset 5 digits may be sequentially selected and loaded in the 5 latches .These 5 digits will be used by the duty cycle controller as it will be explained later.

After finishing this if C2 is pressed once more Y5 will go low keeping the digital output data from the latches unchanged. For changing this data the master reset switch S3 must be pressed and the sequence is repeated once more. Y5 will be used as the trigger of the 555 timer circuit to start the On time interval of the power switch.

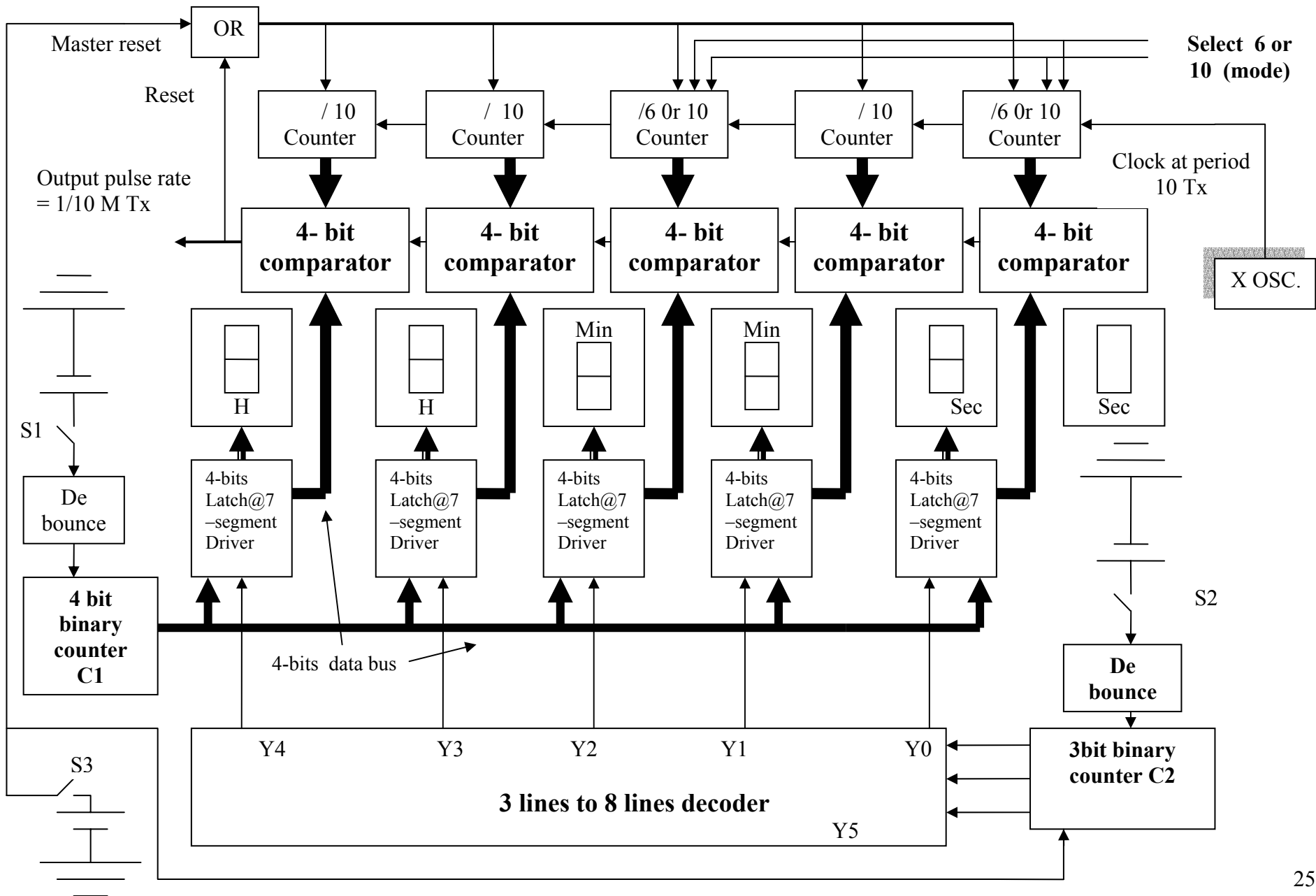


Fig.2.2 Circuit details for the module control circuits

## II-4 THE DISPLAY

This part Contains:

- Five 7-segments decoder / driver common cathode type SN 74248.
- 6 common cathode 7- segment display type MAN 7272.

The display will be used when time is selected in either format .The first digit from right always displays 0 since the time resolution is either 10 ms or 10 seconds. The decimal point indicator on each digit is used to give the status of the associated latch circuit. The decimal point LED of each display unit is connected to the corresponding Y output from the decoder, then if this LED is off it means that the corresponding latch is transparent and we can access and change this digit. Of course only one decimal point LED is ON at a time. When ms mode is selected the display will give the time interval in ms ; **example :** 06 42 10 this means that the time is sixty four thousands two hundreds ten ms = 64.21 s .

In the H M S mode if the display shows: 01 25 20 , this means that the time interval is 1 hour , 25 minutes and 20 seconds.

## II-5 THE DUTY CYCLE CONTROLLER.

This part Contains:

- Five 4 bit comparators type SN 4785 MSI IC chips
- Six 4 bit counter type SN 4790 MSI IC chips
- One OR gate type SN 7432 IC chip
- One J-K FF type SN 7473 IC chip
- One D- type FF SN 7474 IC chip

- One X-OR gate SN 7486 IC chip
- 1 M Hz crystal oscillator.

The circuit operation is as following:

The 5-comparators are cascaded, to compare two 5-digit numbers. The first 5- digits number input to the cascaded comparators is the latch circuits outputs which are the same as that displayed, actually this number represents the value M given in equation 2.1. The second 5- digits number is obtained by cascading five 4- bits decade counters ( 7490) . These cascaded counters are clocked from the crystal oscillator whose frequency is divided by 10 to produce a trigger pulses with period  $= 10T_x$  as explained in section II-2. This 5- digit decade counter when reset starts counting from 00000 to 99999 , but when its count reaches the value written by the latch circuits (M), the equality output from the last stage of the comparators goes high. This signal is used to reset the counters and hence restart another comparison circuit. The pulse rate of this equality signal is then:

$$\text{Pulse rate of equality signal} = f_x/10M \quad (2.4)$$

This signal is used to trigger a j-k FF to produce a 50% duty cycle waveform at rate  $f_x/20M$ . As shown in Fig.2.3 the output from the J-K FF is delayed with delay time  $10 T_x$  using a D-type FF. The 50% duty cycle signal is then X-ORED with the delayed one to produce a rectangle waveform its ON time is  $10 T_x$  and its period is  $10M T_x$  then we may write the duty cycle of this signal as:

$$d = 1/M \quad (2.5)$$

Equation 2.5 shows that the above described circuit can produce exactly the signal needed by the SSC.

In the H M S mode the counter configuration has to be modified to meet this time mode. Like a personal watch the counter sequence becomes 23 59 59. This may be achieved by simply reset the first and third counters from right if their count reaches 6. Of course this will be activated only when the H M S mode is selected. A complete timing diagram is given in Fig. 2.4

## II-6 OPERATING SEQUENCE

- 1- Select the time range ms OR H M S Using S0
- 2- After power On press S3 to reset all counters and latches D4 is Off in this time.
- 3- Press and release S1 to enter the most significant digit in the display
- 4- Press S2 once again D3 will be off then enter the next digit by .  
Pressing and releasing S1
- 5- Repeat step 4 3 times more to enter the next 3 digits.
- 6- Repeat steps 1 to 7 to change time setting.
- 7- To start the timer you have to be at step 7, press S2 once will trigger the 555 circuit and start the time interval.
- 8- To stop the timer manually press the reset switch S1

**Notice that the first digit of the display from right is always displaying Zero because the step is either 10 ms or 10 sec.**

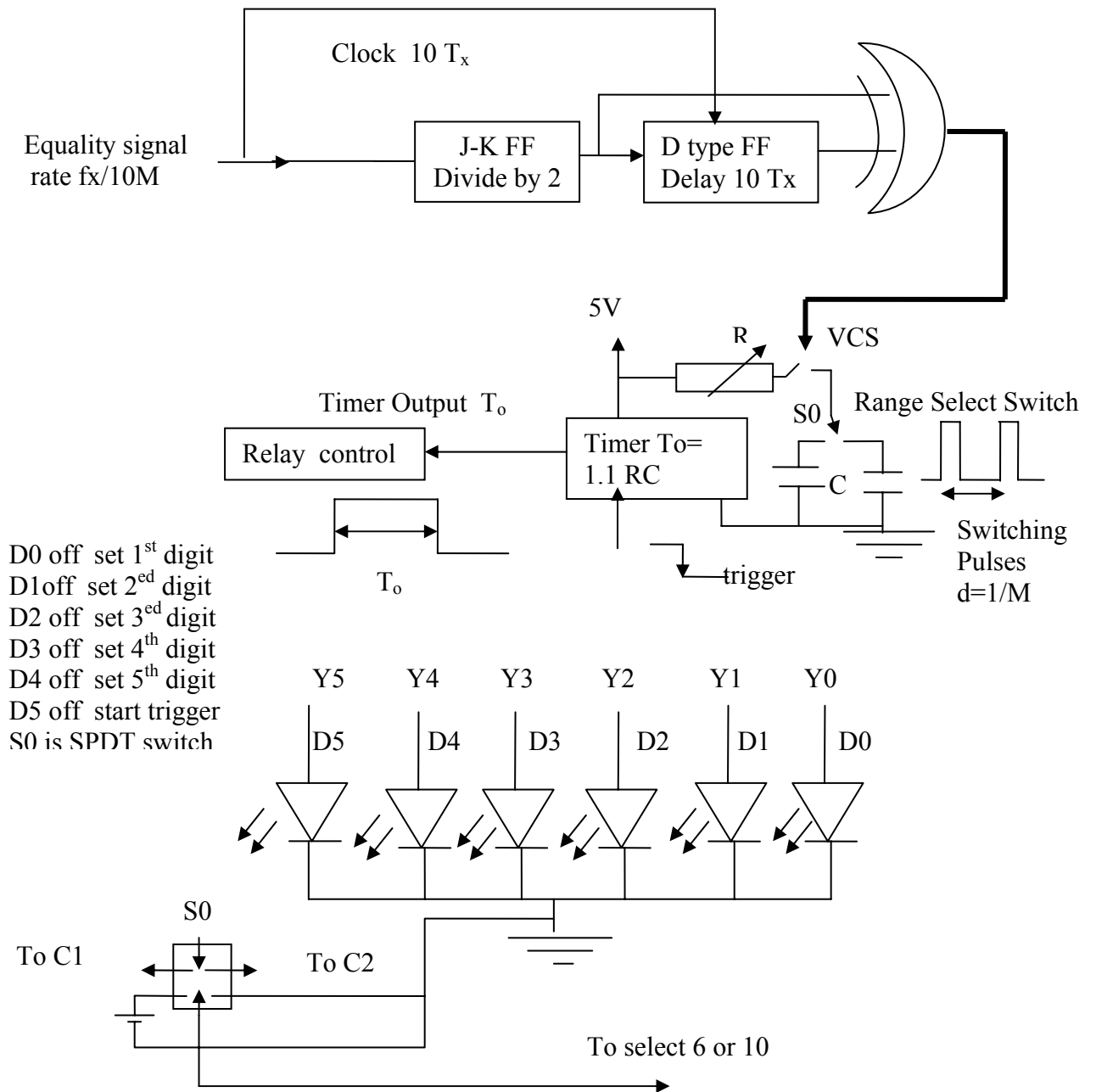


Fig. 2.3 Switching and timer circuit

**Notice that only one LED is off at a time**

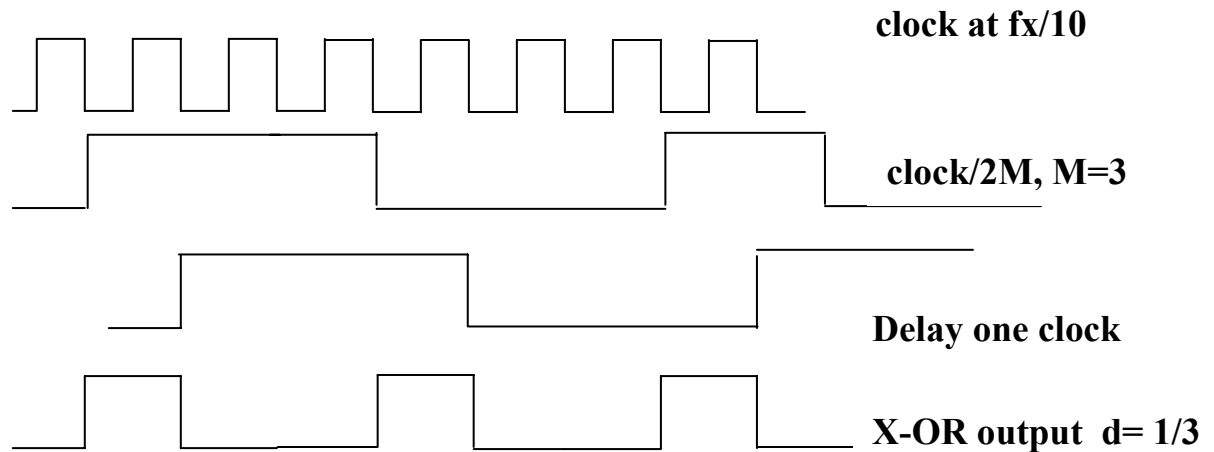


Fig.2.4 Timing diagram for variable duty cycle switching signal

## II-7 EXPERIMENTAL WORK

The system described above had been completely built and tested at the laboratory. All the circuits including the power relay are powered from a single 5V dc power supply.

The circuit of the dc power supply is the traditional one that employs

- 110-220/ 0-9 volt 1 A transformer
- 2 A bridge rectifier,
- 1000  $\mu$ F smoothing capacitor and
- Single 5V / 1.5 A voltage regulator IC chip type 7805

The measured dc current supplied to the circuit was about 930 mA with a total power consumption of  $5 \times 0.93 = 4.65$  W.

The circuit was tested for several time intervals and confirms the theoretical analysis. Typical waveforms for both the switched capacitor charging waveforms and the output time pulse from the timer are given below for different time intervals. In order to get a stable and fixed waveforms like that given by Fig 2.4 a,b,c,d the circuit was periodically

triggered at a suitable rate to show both signals . The switched capacitor charging discharging cycle is very clear where one can recognize the charge and stop times of the capacitor. Extra time intervals cannot be recorded but can be measured using external precise stop watch triggered as the same instant.

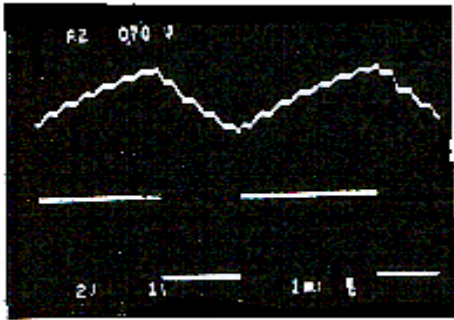


Fig. 2.5-a  
 Upper : Switched capacitor waveform  
 Lower: Output pulse  $T_o = 30$  ms  
 Time base X 10

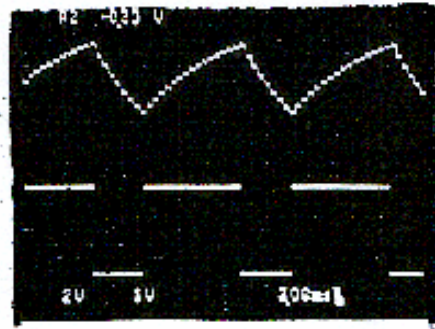


Fig. 2.5-b  
 Upper : Switched capacitor waveform  
 Lower : Output pulse  $T_o = 60$  ms  
 Time base X 10

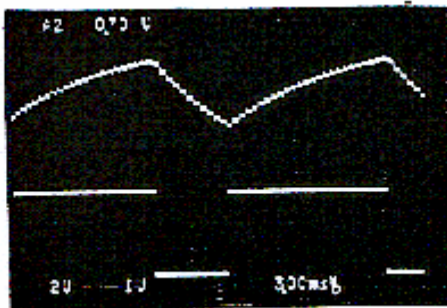


Fig. 2.5-c  
 Upper : Switched capacitor waveform  
 Lower : Output pulse  $T_o = 80$  ms  
 Time base X 10

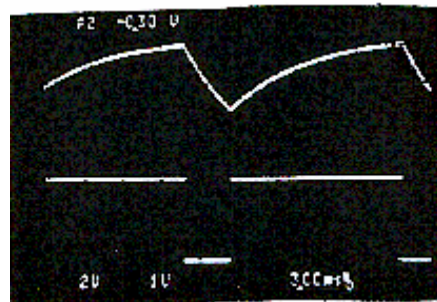


Fig. 2.5-d  
 Upper : Switched capacitor waveform  
 Lower : Output pulse  $T_o = 100$  ms  
 Time base X 10

## **CHAPTER III**

### **THE $\mu$ - CONTROLLER BASED TIMER**

#### **III-1 INTRODUCTION**

The main objective of this project is to develop a low cost timer module that may be fabricated locally, and meets most of the features available in the international market. The control circuit described in the previous chapter suffers from the disadvantages of being, large size, high cost, and high power consumption. The overall control circuit in addition to the other added features like display drivers , control, and data entry ...etc may be implemented on a single VLSI chip using FPGA ( Field Programmable Gate Array) or other programmable technology, such as low cost microcontrollers, according to the cost and the available tools. This new technologies becomes today the best solution for implementing digital system on single chip without going through the complex process of developing a special purpose IC. Digital design using programmable Logic devices (example FPGA)) or microcontrollers is a cost effective way to save time, cost and get high system performance as regarding added features, power consumption, sizing and reliability. A comparative analysis between FPGA and  $\mu$ -controllers was done in order to select favorite one of them for implementation. The analysis results are summarized in table 3-1

Based on the above table we decided to use the  $\mu$ -controller type AT89C2051. The details and features of this  $\mu$ -controller will be given in the next section.

Table 3-1 A comparative analysis between FPGA and  $\mu$ -controllers

Comparison parameter	FPGA	$\mu$ -controller Type AT89C2051
Size	Similar or more	Similar or less
Cost / unit	More than 15U\$	Less than 10U\$
local Availability	Can be supplied	Available easily
Power consumption	Low	Very low
Programmability	Easy	Very easy
Price of programming tool (HW)	Cheap	Very cheap
Price of programming software	High	Free from internet
Reliability	Reliable	Highly reliable

### III-2 THE $\mu$ -CONTROLLER TYPE AT89C2051

The AT89C2051 is a low-voltage, high-performance CMOS 8-bit microcomputer with 2K bytes of Flash programmable and erasable read only memory (PEROM). The device is manufactured using Atmel's high density nonvolatile memory technology and is compatible with the industry-standard MCS-51 instruction set. By combining a versatile 8-bit CPU with Flash on a monolithic chip, the Atmel AT89C2051 is a powerful microcomputer which provides a highly-flexible and cost-effective solution to many embedded control applications.

The AT89C2051 provides the following standard features:

- 2K bytes of Flash, 128 bytes of RAM,
- 15 I/O lines, two 16-bit timer/counters,

- A five vector two-level interrupts architecture,
- A full duplex serial port,
- A precision analog comparator,
- On-chip oscillator and clock circuitry.

In addition, the AT89C2051 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port and interrupt system to continue functioning. The power-down mode saves the RAM contents but freezes the oscillator disabling all other chip functions until the next hardware reset. The circuit needs only a crystal oscillator and 10 $\mu$ F capacitor to make soft reset with power on.

The design is optimized in order that we use minimum external components to build the timer system described in chapter II with the same specifications. The circuit diagram for the whole system is given in Fig3.1 where we recognize that the external components around the  $\mu$ -controller is only 2 CD4066 analog switch and the 555 timer with its associated resistor and capacitors elements. Only one push button de-bounced switch is used for all functions.

The circuit operates as follows:

- 1- With turning the power on all the  $\mu$ -controller registers are reset to their initial values defined in the data sheets.
- 2- The 89C2051 is programmed to wait for 5 secs after power reset, during this period if S is pressed once and released, the time mode is changed to H M S mode; otherwise the default mode is the ms mode. An indicator green LED illuminate when H M S mode is selected.

- 3- The controller is now ready for entering the time interval by the user. The user starts by entering the most significant digit (the most left one). The corresponding seven segment unit is enabled waiting for S to be pressed. When this later is pressed and kept pressed this digit will start incrementing from 0 to 9. It takes about 1 sec for each increment, and it stops if S is released. So the user has to release S at the desired value for this digit.
- 4- When S is released the program enables the next digit from left and stores the equivalent binary value of the previous digit into the data memory.
- 5- The user repeat steps 3 and 4 five times until he enters the 5 digits representing the time interval in either format.
- 6- When releasing S for the last time the display will display the interval the user had entered, and the program will process the stored data and generates the periodic switching signal needed by the SSC and with the suitable duty cycle d.
- 7- To trigger the 555 timer circuit S is pressed once more and released, the controller will then disable the display , trigger the 555 timer and goes into endless loop that produce the periodical switching signal of the SSC.
- 8- To change the time interval or stop the timer the power must be switched off and On, and the user repeats steps 2 to 7 to re-enter the new value.

More details will be given in the next section.

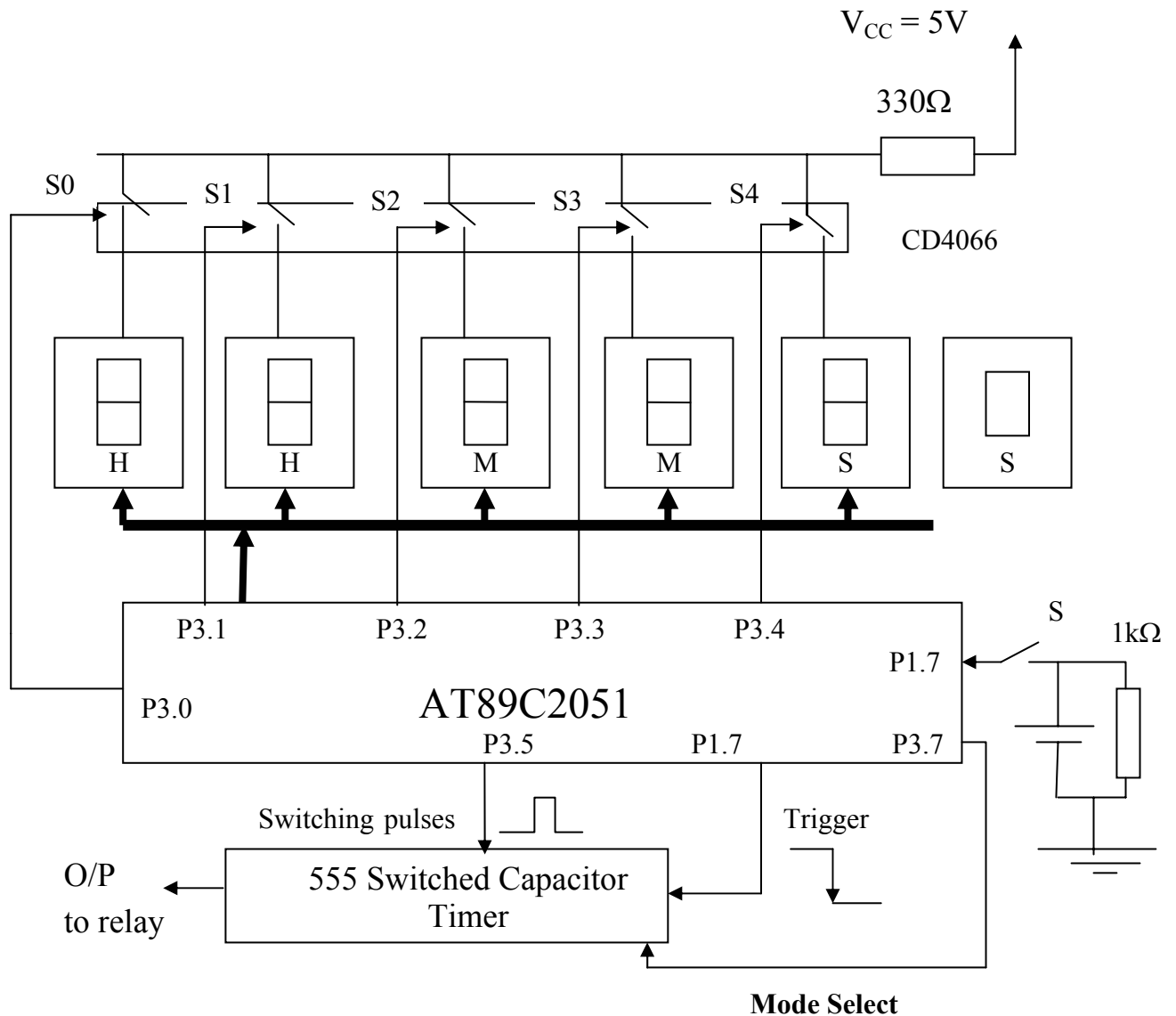


Fig.3.1 Circuit diagram

### III-3 CIRCUIT DESCRIPTION & OPERATION

Referring to Fig. 3.1 the first 7 bits of port 1 of the At89C2051 (**P1.0 to P1.6**) are connected directly to 7 cathodes of the five 7 segments display units. Each unit of the display is connected to the 5 V supply through an analog switch type Cd4066 in order to individually access each of them. The control signals for the analog switches S0, S1, to S4 are the bits P3.0, P3.1, to P3.4 respectively. This connection allows us to display the

decimal numbers from 0 to 9 sequentially on each unit while blanking the others. The BCD codes of the numbers from 0 to 9 are stored in the  $\mu$ - controller memory in a 10 bytes array length from address 20H to 29H. When P3.0 is set to 1 and S is pressed the program will output the contents of this array sequentially on port 1, the first digit from left will display the numbers from 0 to 9 with about 2 sec interleaving time. The user has to release S at the desired value. When this later is released the program will rotate to right the contents of port P3 to set p3.1 and allow accessing of the second digit from left by pressing S again. This procedure is repeated 5 times until the 5 digits are being selected and their corresponding binary codes for each decimal value are stored in predefined places in the memory. Table 3.2 gives the contents of the memory array 20 h to 29H and the corresponding binary and decimal values.

Notice that the MSB of the BCD is always 1 since only 7 bits are used (P0.0 to P0.6) and P0.7 is used to input the status of S.

Table 3-2 The contents of the memory array 20 h to 29H and the corresponding binary and decimal values.

Address	Decimal value	BCD code abcdefg	Equivalent Hex
20 H	0	1 0000001	81
21 H	1	1 1001111	CF
22 H	2	1 0010010	92
23H	3	1 0000110	86
24H	4	1 1001100	CC
25H	5	1 0100100	A4
26H	6	1 1100000	E0
27H	7	1 0001111	8F
28H	8	1 0000000	80
29H	9	1 0001100	9A

Notice that abcdefg is the segment assignments of the 7- segment LED display as given by Fig3.2.

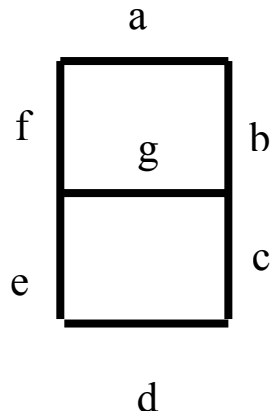


Fig3.2 Segment assignment for 7- segment LED display

After finishing the data entry for the 5 digits the program goes into an endless loop that display the whole 5 digit numbers by time multiplexing the stored BCD data at about 30 Hz rate. This loop can only be terminated if S is pressed once; at this moment the program goes into another endless loop that generates the switching pulses at the desired duty cycle and use P3.5 to output this signal to the SSC in the timer circuit. Just after releasing S the program will send a negative trigger pulse to the timer to start its time interval. The program will keep this loop until it is reset by switching the power off and On. Now it is ready to receive a new data entry from the user.

#### **III-4 THE MODE SELECT SIGNAL.**

This signal is produced by the  $\mu$ - controller during the next 5 sec starting after power reset. This signal taken from P3.7 which is cleared to 0 (low) if S is pressed during the next 5 second from any power reset other wise it is kept 1 (high). If P3.7 is 0 the H M S mode is selected while if P3 .7 is kept 1 the ms mode is selected. A green LED is wired

at this output to acknowledge the user about the selected mode. Notice that we have to keep this value unchanged during a given run of the program. In the timer circuit this signal is used to connect the suitable capacitor as shown in Fig.3.3. A single pole double through (SPDT) switch is wired using two analog switches type CD4066 IC chip, when P3.7 is low the 10  $\mu$ F capacitor is connected which makes the time incremental = 10 sec as given in section II-2. The other capacitor 10 nF gives the ms range.

### III-5 THE SWITCHING SIGNAL

The switching signal is generated as a periodical rectangle signal with variable duty cycle. The On period  $T_1$  is fixed while the off period depends on the values entered by the user and is equal to  $(M-1) T_1$ , where M is a count number calculated by the program as follows:

For the ms time mode, assume that the input data digits are  $D_5 D_4 D_3 D_2 D_1$  then  $M = D_1 + 10 D_2 + 100D_3 + 1000D_4 + 10000D_5$

$$M = D_1 + (D_2 + 10 D_3) 10 + (D_4 + 10D_5) (10) (100) \quad (3.1)$$

For the H M S time mode:

Second	Minute	Hours	
$D_1$	$(D_2 + 10 D_3) 6$	$(D_4 + 10 D_5) (6) (60)$	(3.2)

The format of equations 3.1, 3.2 explains how this time intervals are implemented using nested counter method in assembly programming of the  $\mu$ - controller. Since the maximum count length is limited to FFH (255) we cannot use the direct value of M in a single delay loop. The delay loop is divided into three nested loops; the lengths of the 3 loops are  $D_1-1$ ,  $(D_2+10 D_3)$ ,  $(D_4+10D_5)$  and always less than 255. In the ms time mode

the first loop of length  $D_1-1$  is repeated once, the second loop of length  $(D_2 + 10 D_3)$  is repeated 10 times while the third of length  $(D_4+10D_5)$  is nested again to be repeated 10 and 100 times. In the H M S time mode the first loop of length  $D_1-1$  is repeated once, the second loop of length  $(D_2 + 10 D_3)$  is repeated 6 times while the third of length  $(D_4+10D_5)$  is nested again to be repeated 6 and 60 times.

**Example**: in the H M S mode the required interval is

{ 01 hr 24 min 30 sec } then :

$$D_1 = 3$$

$$D_2 = 4$$

$$D_3 = 2$$

$$D_4 = 1$$

$$D_5 = 0$$

$$M = 3 + 24 (6) + 1 (6) (60) = 507$$

And the total time interval in sec = 5070 secs

### **III- 6 THE ASSEMBLY PROGRAM**

In order to impalement the operating procedure described in the above sections an assembly program had been developed and tested by two methods:

First by simulation using the MA-51 macro assembler, (Copyright RAISONANCE S.A), this software is specially assigned for simulating assembly program for most of the  $\mu$ -controller having 8051 core structure.

Second: by a complete hardware implementation for the circuit given by Fig.3.1, where real time signals can be traced and verified.

The experimental work confirms the simulation and the circuit works properly. In order to follow up the assembly program a flowchart is given below while the complete assembly program is given in appendix A. Appendix B contains the data sheets for all components given in Fig.3.1.

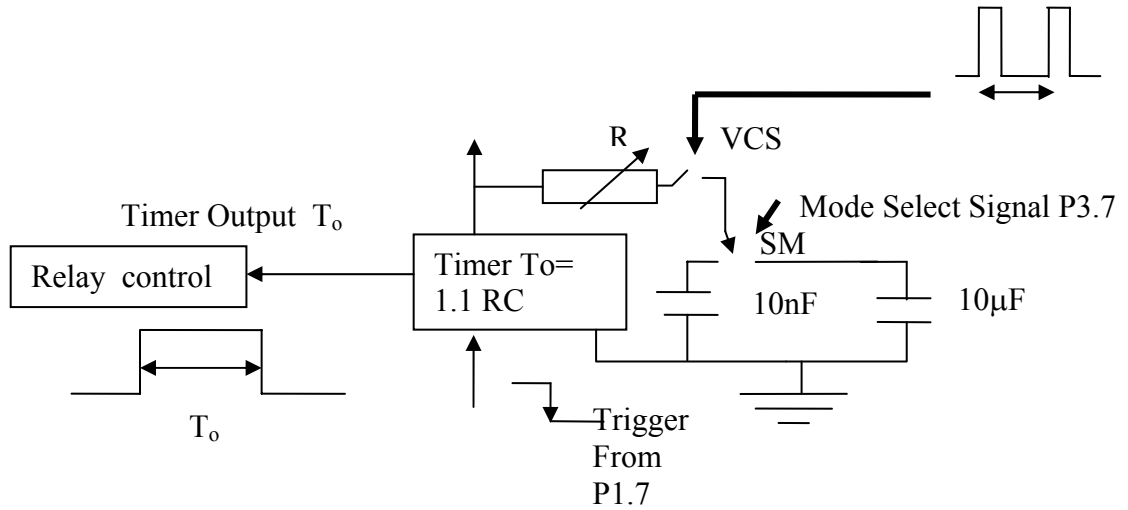
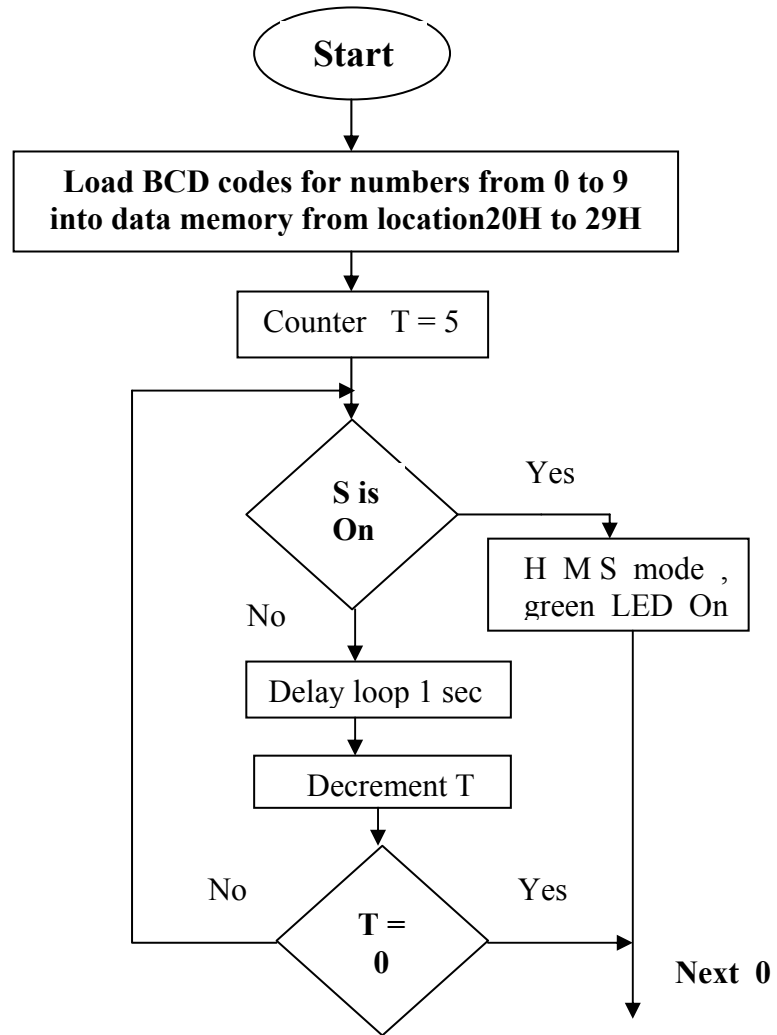
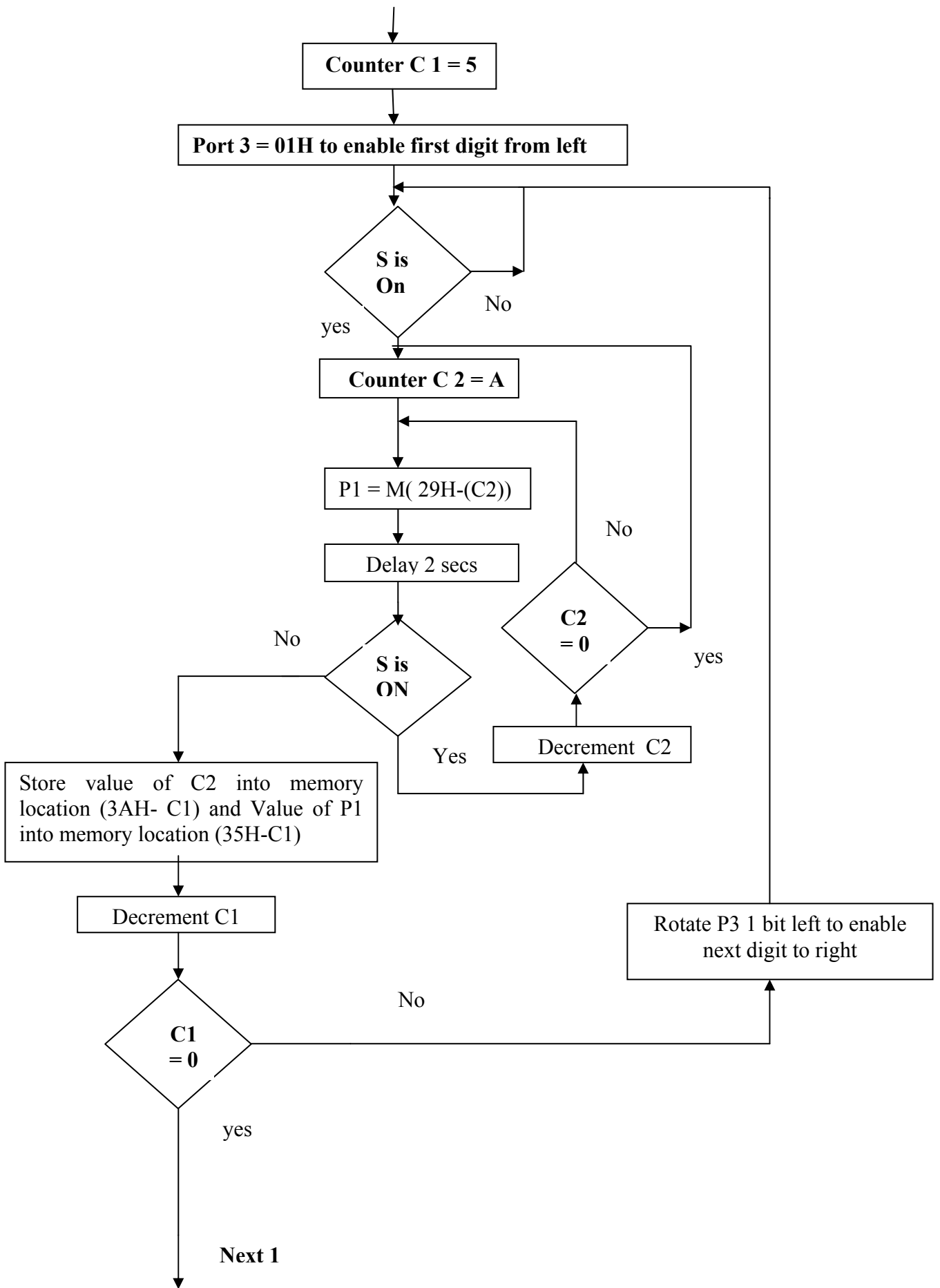
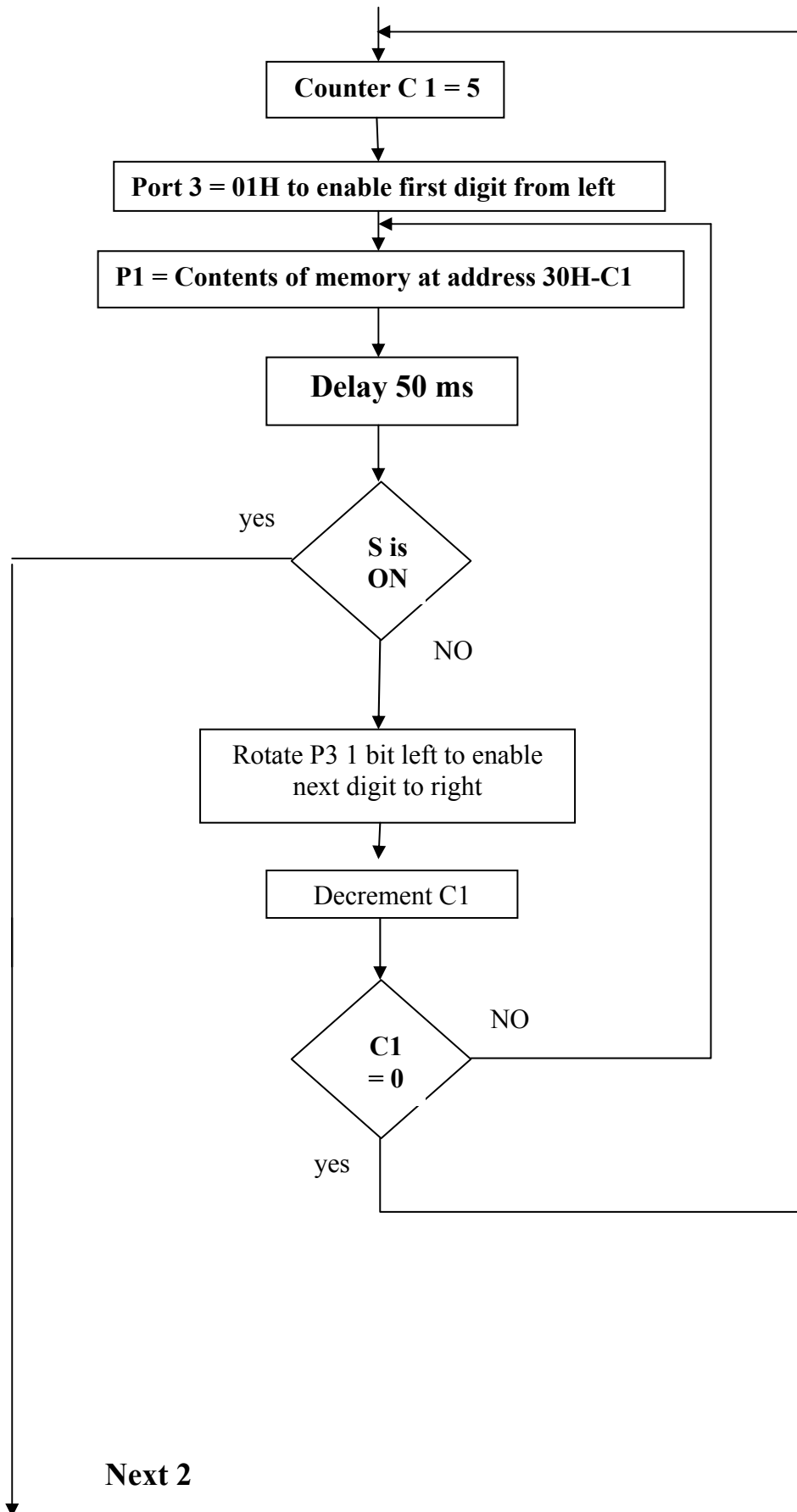


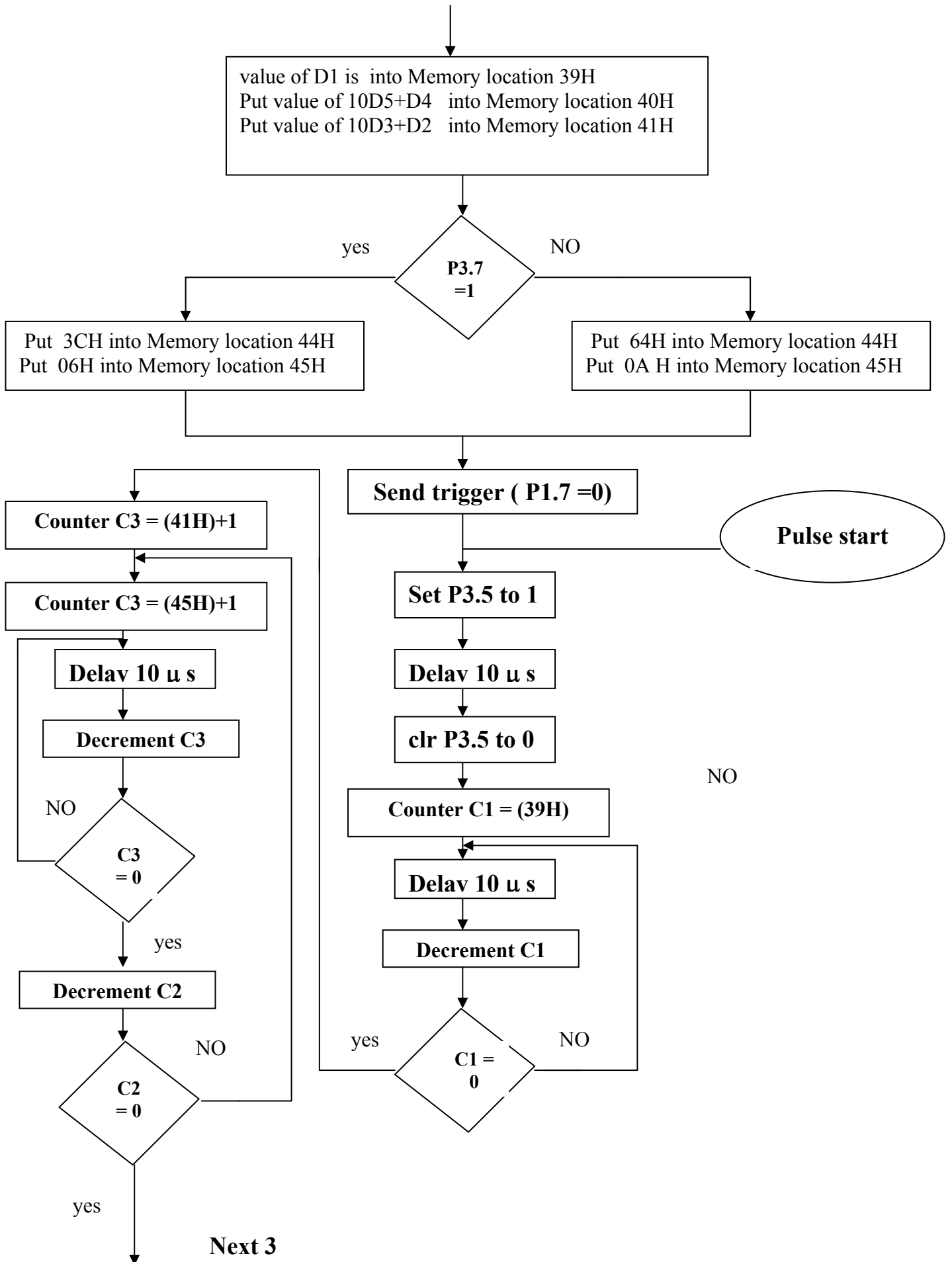
Fig. 3- Timer circuits and its control signals

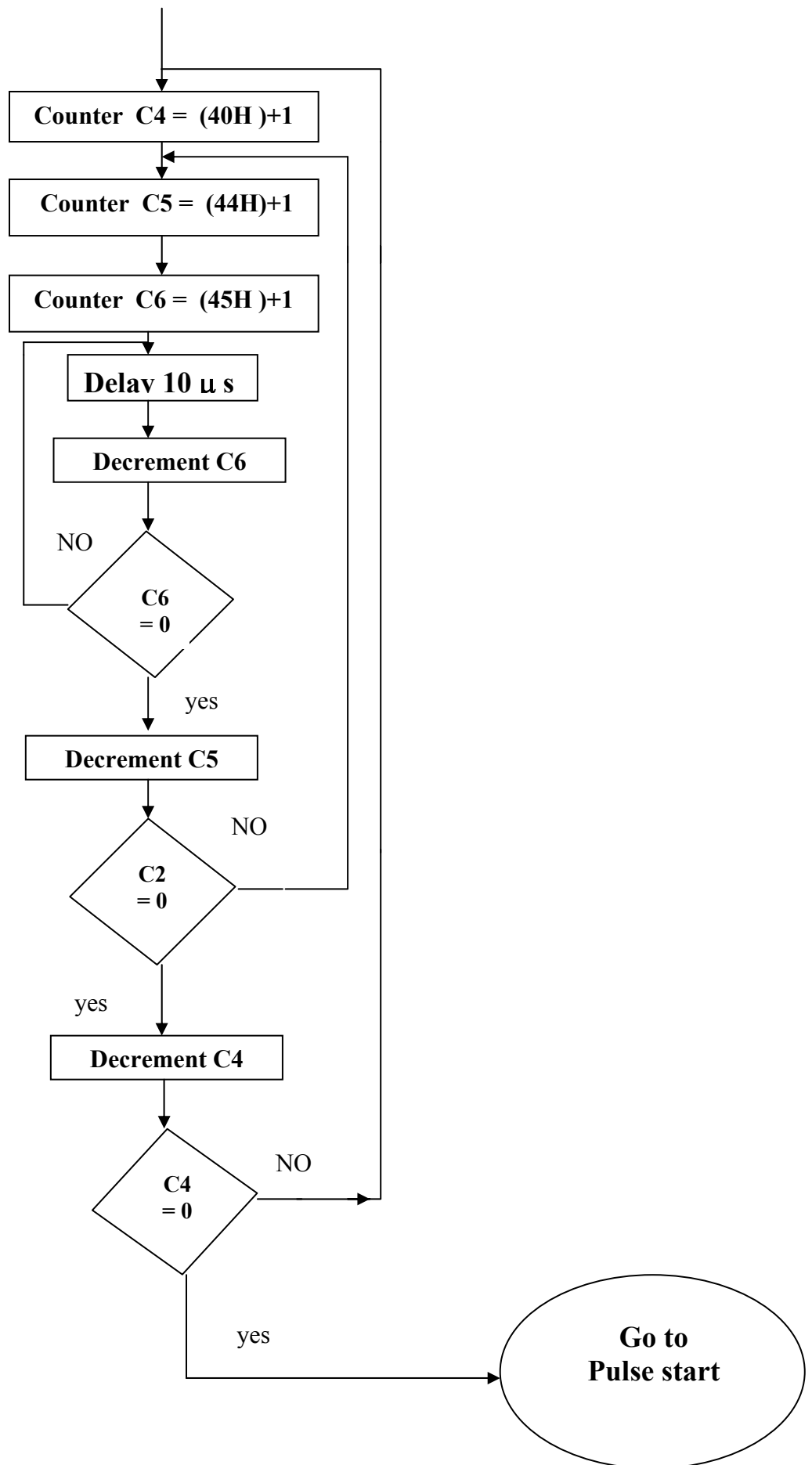
The flowchart











## **Summery of the flow chart:**

<b>Flowchart section</b>	<b>Function</b>
<b>Start to next 0</b>	<b>Input BCD codes and determine time mode</b>
<b>Next 0 to Next1</b>	<b>Enter and store the 5 data digits D<sub>1</sub>, D<sub>2</sub>, D<sub>3</sub>, D<sub>4</sub>, D<sub>5</sub></b>
<b>Next 1 to Next2</b>	<b>Display data on 7- segment display</b>
<b>Next 2 to Next3</b>	<b>Data processing and switching pulses generation</b>

Notice that the program will continue producing the switching pulses with the same selected duty cycle until it receives an external reset or power off.

### **III-7 EXPERIMENTAL WORK**

The system described above was completely built and tested at the laboratory. All the circuits including the power relay are powered from a single 5V dc power supply. The circuit of the dc power supply is simple, low cost and small size ,since the circuit needs only few mAs. The circuit is shown in Fig 3.4

- 0.68  $\mu$ F ceramic capacitor 250 V
- 0.5 A bridge rectifier,
- 1000  $\mu$ F smoothing capacitor and
- Single 5V / 0.5 A voltage regulator IC chip type 7805

The reactance  $X_c$  of the 0.68  $\mu$ F ceramic capacitor at 60 Hz equals:

$$X_c = 10^6/120\pi*0.68 = 3903 \Omega$$

The current passing through  $X_c$  is about 50 mA (RMS value) which makes about 200 V (RMS value) voltage drop across it. The voltage applied at the input of the bridge rectifier is then about 20 V (RMS value) which is reasonable. This technique is usually

used when the dc load needs few and fixed current, in this case the series capacitor value can be estimated and use to divide the voltage with the bridge to avoid the need of step down transformer.

The measured dc current supplied to the circuit was about 30 mA with a total power consumption of  $5 \times 0.03 = 0.15$  W.

The circuit was tested for several time intervals and confirms the theoretical analysis.

### III-7.1 Cost

The cost of the timer module employing the  $\mu$ - controller can be calculated using component price table 3-3 .

Table 3-3 component price table

<b>Item description</b>	<b>Unit Price / SR</b>	<b>Total / SR</b>
<b>1 X <math>\mu</math>- controller Atmel 89C52</b>	<b>30</b>	<b>30</b>
<b>2X CD 4066 Analog switch</b>	<b>3</b>	<b>6</b>
<b>1X 555 Timer</b>	<b>3</b>	<b>3</b>
<b>6 X 7 segment display</b>	<b>4</b>	<b>24</b>
<b>1 Bridge rectifier</b>	<b>3</b>	<b>3</b>
<b>1X 7805 regulator</b>	<b>3</b>	<b>3</b>
<b>Passive components</b>	<b>5</b>	<b>3</b>
<b>Printed circuit fabrication</b>	<b>20</b>	<b>20</b>
<b>Total cost</b>	<b>-----</b>	<b>92 SR</b>

It is to be noted here that, the total cost is about 25 US\$ , although this cost is at least half price of the most cheapest timer modules in the market , it can be reduced to less than 10 US\$ if components are bought in gross and fabrication is done in mass production.

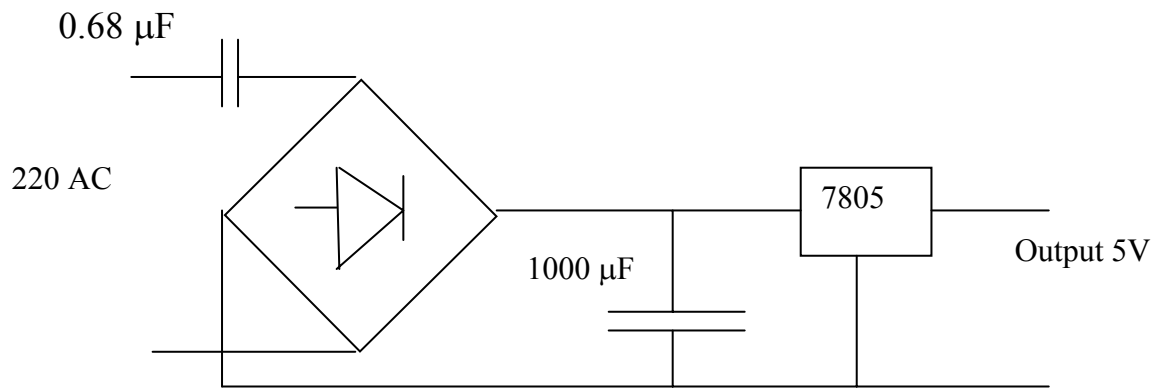


Fig.3.4 DC power Supply

## CONCLUSION

Timers are widely used in so many industrial and commercial applications. Single IC chip with external timing resistors and capacitor may implement the timer function. The use of SSC with timer circuits extends their capabilities as regarding the operating range and the time/ frequency control method. Digital programming is possible and accurate with the help of advanced programmable circuit like microcontrollers.

The design of a digitally controlled duty cycle pulse generator circuit is presented and analyzed. The mathematical model shows a direct relation between the time interval and the switching duty cycle. Two time modes are available where the user can select either ms time mode or H M S time mode. In either modes the entered number is processed to adjust the duty cycle of the switching signal .The approach presented in chapter II uses the available off- shelf digital SSI and MSI IC,s. Although this approach is not the optimal as regarding cost and size, it had been used to optimize the design as regarding the system functions like the user interface, the display ...etc, and also to get an optimal definition for the logic sequence, signals and data processing. Circuit details as well as logic operation had been explained. The operating sequence is optimized for simple and direct setting of time intervals. The circuit had been completely built and tested, where the experimental results confirm the theoretical analysis.

A complete design for the timer module is given and analyzed in chapter III. The circuit components needed to impalement the duty cycle controller had been replaced by a single 20 pins IC Chip. This chip is the Atmel 89C52  $\mu$ - controller where an assembly program was developed to realize all the logic operation described and approved by the discreet circuit. The circuit uses only one push button switch for all control operations.

The 555 timer circuit and the power relay is the same as described in chapter II. A detailed flowchart was given to explain the sequence of the assembly program. The total power consumption as well as the circuit size are very small and in the same order of commercial timers in the international market. The cost of the presented version is about 25US\$ which is almost half price of the cheapest timer modules in the market. It can be reduced to less than 10 US\$ if components are bought in gross.

The experimental results ensure the efficiency and reliability for implementing accurate and precise timer modules for industrial and commercial applications using SSC in timer circuits.

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**Appendix A  
Program List**

**; Timer 1 Sample program for starting timer job**

**=====**  
**=====**

**; Aim : Display BCD Numbers on 7 segment display and  
; produce variable duty cycle pulses**

**-----**  
**\$include(REG51.inc)**

**-----**

**MOV 20H,#081H  
MOV 21H,#0CFH  
MOV 22H,#092H  
MOV 23H,#086H  
MOV 24H,#0CCH  
MOV 25H,#0A4H  
MOV 26H,#0E0H  
MOV 27H,#08FH  
MOV 28H,#080H  
MOV 29H,#09AH**

**MOV R2,#0FFH  
DEL1:  
MOV R1,#0FFH  
DEL:  
NOP  
NOP  
NOP  
NOP  
NOP  
NOP  
NOP  
NOP  
NOP  
NOP  
NOP  
NOP  
NOP  
DEC R1  
MOV A,R1  
JNZ DEL  
DEC R2  
MOV A,R2  
JNZ DEL1**

```

MOV 50H,P1
MOV A,#0FEH
ANL A,50H
MOV P3,A
MOV R4,#05H
Loop3:
MOV R0,#20H
Switch:
JNB P1.7,CON
SJMP Switch
CON:
MOV P1,@R0
MOV R3,#01H
Loop2:
MOV R2,#0FFH
Loop1:
MOV R1,#0FFH
Loop:
NOP
NOP
NOP
NOP
NOP
NOP
NOP
NOP
NOP
NOP
NOP
DEC R1
MOV A,R1
JNZ Loop
MOV P2,R2
DEC R2
MOV A,R2
JNZ Loop1
DEC R3
MOV A,R3
JNZ Loop2
JB P1.7,OK
INC R0
MOV A,#29H

```

```

XRL A,R0
JNZ CON
SJMP Loop3
OK:
MOV A,#35H
SUBB A,R4
MOV R1,A
MOV @R1,P1
MOV A,#3AH
SUBB A,R4
MOV R1,A
MOV A,R0
SUBB A,#20H
MOV @R1,A
MOV A,P3
ORL A,#080H
RL A
ANL A,50H
MOV P3,A
DEC R4
MOV A,R4
JNZ Loop3
NOP
NOP
NOP
NOP
NOP
Disp1:
MOV A,#0FEH
ANL A,50H
MOV R5,A
MOV R4,#00H
Disp3:
MOV A,#30H
ADD A,R4
MOV R1,A
MOV P1,@R1
MOV P3,R5
MOV
Disp:
NOP

```

**NOP**  
**NOP**  
**NOP**  
**NOP**  
**NOP**  
**NOP**  
**NOP**  
**DEC R2**  
**MOV A,R2**  
**JNZ Disp**  
**MOV A,P3**  
**ORL A,#080H**  
**RL A**  
**ANL A,50H**  
**MOV R5,A**  
**INC R4**  
**MOV A, R4**  
**SUBB A,#05H**  
**JNZ Disp3**  
**JNB P1.7,ST**  
**SJMP Disp1**  
**ST:**  
**MOV P3,#0FFH**  
**MOV B,#0AH**  
**MOV A,35H**  
**MUL AB**  
**ADD A,36H**  
**MOV 40H,A**  
**MOV A,37H**  
**MOV B,#0AH**  
**MUL AB**  
**ADD A,38H**  
**MOV 41H,A**  
**MOV A,50H**  
**ANL A,#80H**  
**JZ MODE**  
**MOV 44H,#64H**  
**MOV 45H,#0AH**  
**SJMP Trigger**  
**MODE:**  
**MOV 44H,#03CH**

**MOV 45H,#06H**  
**Trigger:**  
**JNB P1.7,PULSE**  
**SJMP Trigger**  
**PULSE:**  
**SETB P3.6**  
**MOV R0,#0AH**  
**ON:**  
**NOP**  
**NOP**  
**DEC R0**  
**MOV A,R0**  
**JNZ ON**  
**CLR P3.6**  
**MOV R1,39H**  
**OFF1:**  
**MOV R0,#0AH**  
**OFF8:**  
**NOP**  
**NOP**  
**DEC R0**  
**MOV A,R0**  
**JNZ OFF8**  
**DEC R1**  
**JNZ OFF1**  
**MOV R1,41H**  
**INC R1**  
**OFF2:**  
**MOV R2,45H**  
**INC R2**  
**OFF3:**  
**MOV R0,#0AH**  
**OFF:**  
**NOP**  
**NOP**  
**DEC R0**  
**MOV A,R0**  
**JNZ OFF**  
**DEC R2**  
**MOV A,R2**  
**JNZ OFF3**

```
DEC R1
MOV A,R1
JNZ OFF2
MOV R1,40H
INC R1
OFF4:
MOV R2,44H
INC R2
OFF5:
MOV R3,45H
INC R3
OFF6:
MOV R0,#0AH
OFF7:
NOP
NOP
DEC R0
MOV A,R0
JNZ OFF7
DEC R3
MOV A,R3
JNZ OFF6
DEC R2
MOV A,R2
JNZ OFF5
DEC R1
MOV A,R1
JNZ OFF4
SJMP PULSE
END
```