NAND Gate

A	B	Y
0	0	1 V_{OH}
0	1	1 V_{OH}
1	0	1 V_{OH}
1	1	0 V_{OL}

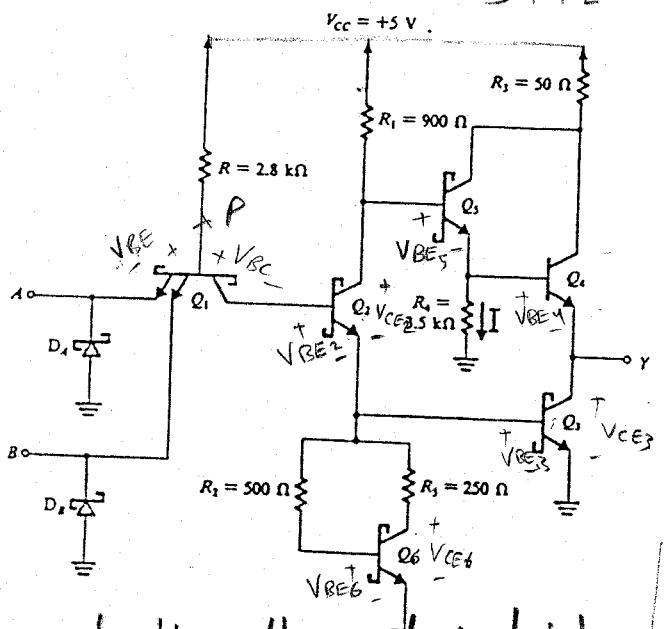
Electrical Engineering Department
EE315 – Digital and Analog Electronic circuits
Summer Session - 1426

4.3/11

H.W# 5

Question : Assume for the shown STTL β_r=0.01 and β=40 .
1- Calculate the voltages at the base of each transistor for V_{OH} and V_{OL}.
2- Calculate the power dissipated by the gate.
3- Calculate the fan-out.

STTL



$\beta = 40$, $\beta_r = 0.01$

① if at least one input low "$V_o = V_{OH}$"
Q.1 on (active)
Q.2, Q.3, Q.6 are off

$V_{cc} = (900) I_{B5} + V_{BE5} + V_{BE4} + V_{OH}$
(very small)

$5 = 0 + 0.75 + 0.7 + V_{OH}$

$\boxed{V_{OH} = 3.55 \text{ Volt}}$

② if all inputs are high "$V_o = V_{OL}$"
Q.1 is (reverse active)
Q.2, Q.3, Q.6 are on
Q.4 is off

$\boxed{V_{OL} = V_{CE3} = 0.35 \text{ Volt}}$

P_H at the all input is high

$I_{B_1} = \dfrac{5 - V_p}{2.8K}$

$V_p = V_{BE3} + V_{BE2} + V_{BC(\text{Inverted})}$
$= 0.75 + 0.75 + 0.75$ or 0.4

$I_{C_2} = \dfrac{5 - V_{C_2}}{900}$

$V_{C_2} = V_{BE3} + V_{CE2}$
$= 0.75 + 0.35$
$= 1.1$

$I_{C_2} = \dfrac{3.9}{900} = 4.33 \text{ mA}$

P_L at the input is low

$I_{B_1} = \dfrac{5 - V_p}{2.8K}$

$V_p = V_{B_1} = V_{BE_1} + V_{E_1} = 1.1 \text{ Volt}$

$I_{B_1} = \dfrac{5 - 1.1}{2.8k} = 1.39 \text{ mA}$

$P_L = 5 \times 1.39m = 6.964 \text{ mW}$

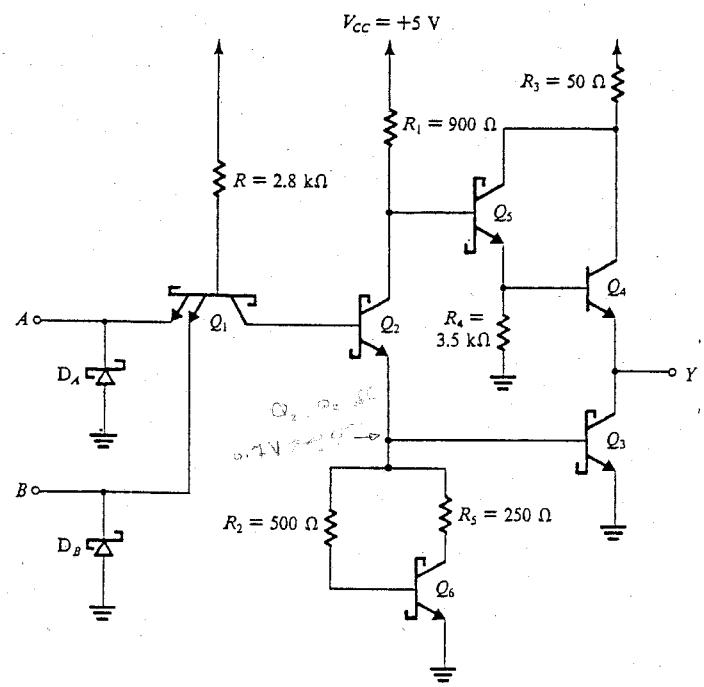


Fig. 14.28 A Schottky TTL (known as STTL) NAND gate.

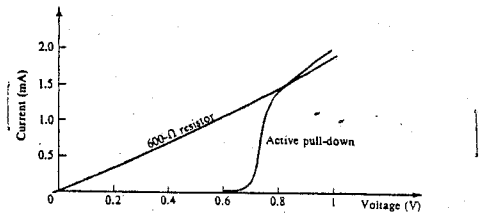


Fig. 14.29 Comparison of the i–v characteristic of the active pull-down with that of a 600-Ω resistor.

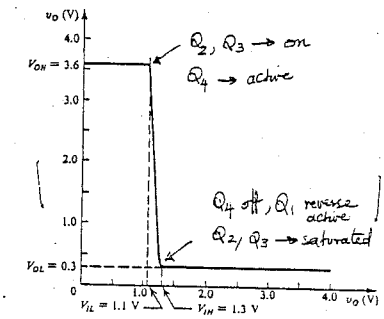
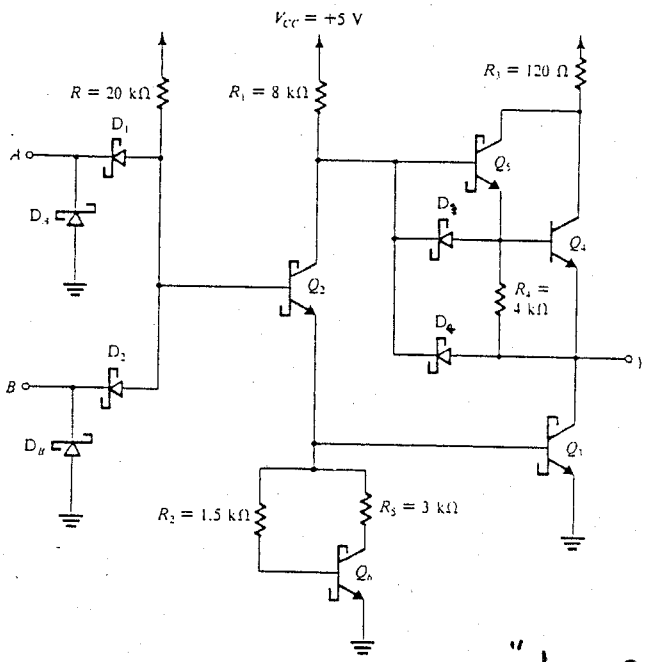


Fig. 14.30 Voltage transfer characteristic of the Schottky TTL gate.



"Low power STTL"

Table 14.1 PERFORMANCE COMPARISON OF TTL FAMILIES

	Standard TTL (Series 74)	Schottky TTL (Series 74S)	Low-Power Schottky TTL (Series 74LS)	Advanced Schottky TTL (Series 74AS)	Advanced Low-Power Schottky TTL (Series 74ALS)
t_P, ns	10	3	10	1.5	4
P_D, mW	10	20	2	20	1
DP, pJ	100	60	20	30	4

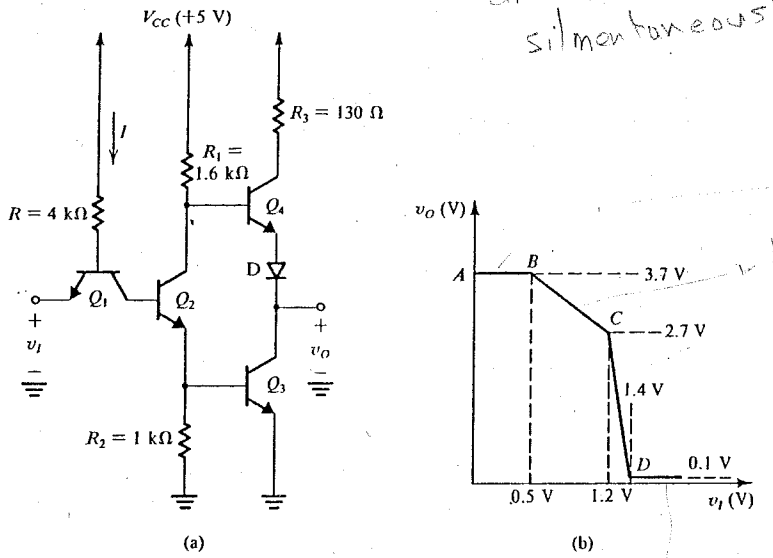


Fig. 14.23 The TTL gate and its voltage transfer characteristic.

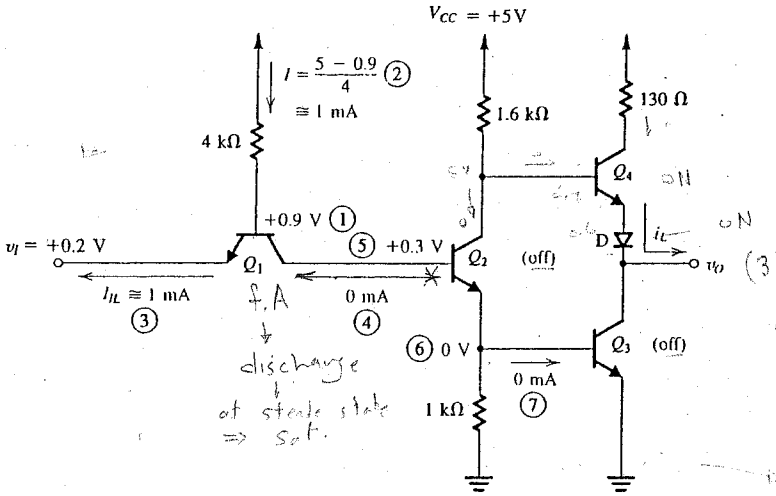


Fig. 14.22 Analysis of the TTL gate when the input is low. The circled numbers indicate the order of the analysis steps.

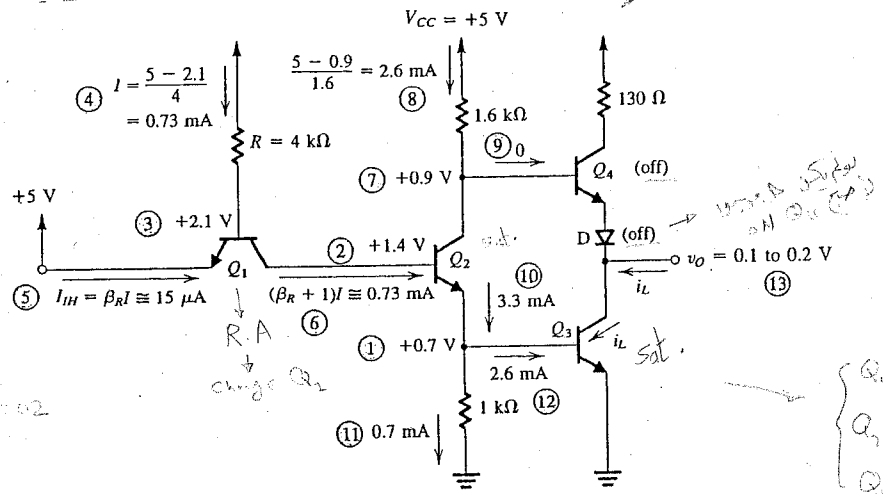


Fig. 14.20 Analysis of the TTL gate with the input high. The circled numbers indicate the order of the analysis steps.

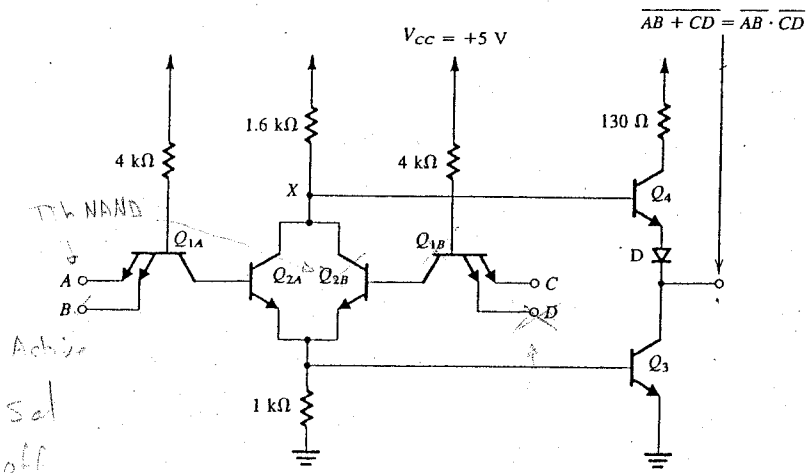


Fig. 14.26 A TTL AND-OR-INVERT gate.