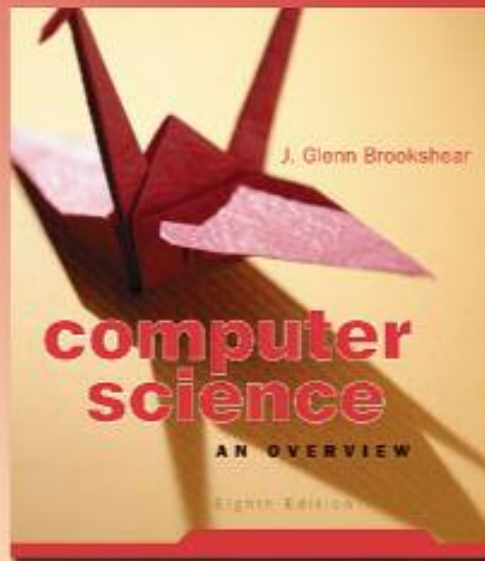


## Chapter 1



## Chapter 1: Data Storage

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## Bits and their meaning

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## Bit patterns

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## Boolean operations

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## Figure 1.1 The Boolean operations AND, OR, and XOR (exclusive or)

### The AND operation

$$\begin{array}{r} 0 \\ \text{AND } 0 \\ \hline 0 \end{array}$$

$$\begin{array}{r} 0 \\ \text{AND } 1 \\ \hline 0 \end{array}$$

$$\begin{array}{r} 1 \\ \text{AND } 0 \\ \hline 0 \end{array}$$

$$\begin{array}{r} 1 \\ \text{AND } 1 \\ \hline 1 \end{array}$$

### The OR operation

$$\begin{array}{r} 0 \\ \text{OR } 0 \\ \hline 0 \end{array}$$

$$\begin{array}{r} 0 \\ \text{OR } 1 \\ \hline 1 \end{array}$$

$$\begin{array}{r} 1 \\ \text{OR } 0 \\ \hline 1 \end{array}$$

$$\begin{array}{r} 1 \\ \text{OR } 1 \\ \hline 1 \end{array}$$

### The XOR operation

$$\begin{array}{r} 0 \\ \text{XOR } 0 \\ \hline 0 \end{array}$$

$$\begin{array}{r} 0 \\ \text{XOR } 1 \\ \hline 1 \end{array}$$

$$\begin{array}{r} 1 \\ \text{XOR } 0 \\ \hline 1 \end{array}$$

$$\begin{array}{r} 1 \\ \text{XOR } 1 \\ \hline 0 \end{array}$$



# Gates

•

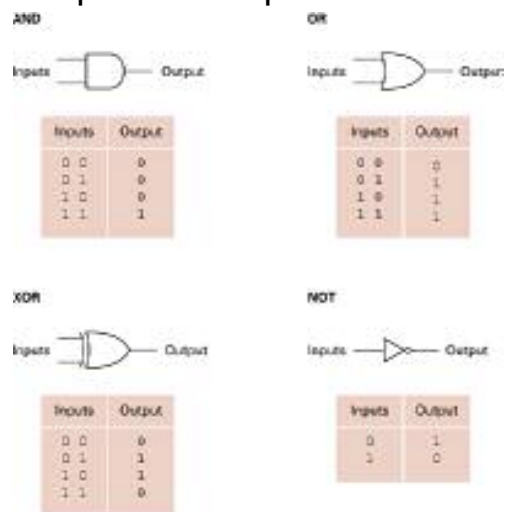
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**Figure 1.2** A pictorial representation of AND, OR, XOR, and NOT gates as well as their input and output values





## storage techniques

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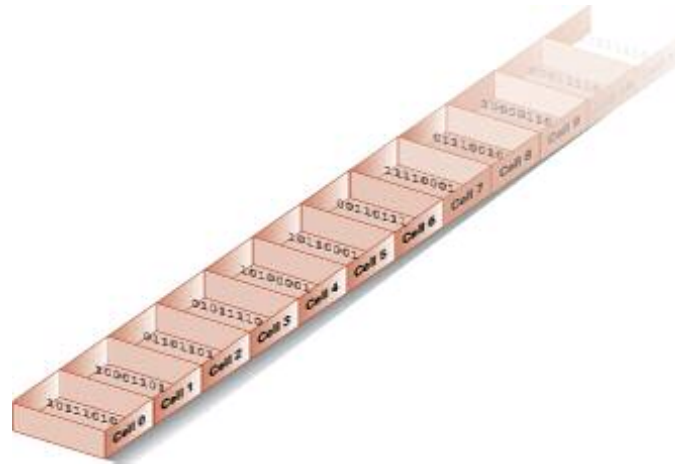
## Main memory: cells

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**Figure 1.8** Memory cells arranged by address



### Measuring memory capacity: Not quite like the metric system

- “ ”
- “ ”
- “ ”

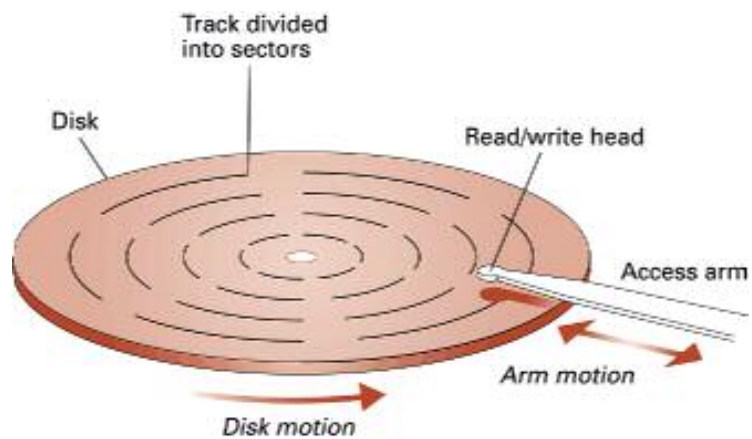


## Mass Storage Systems

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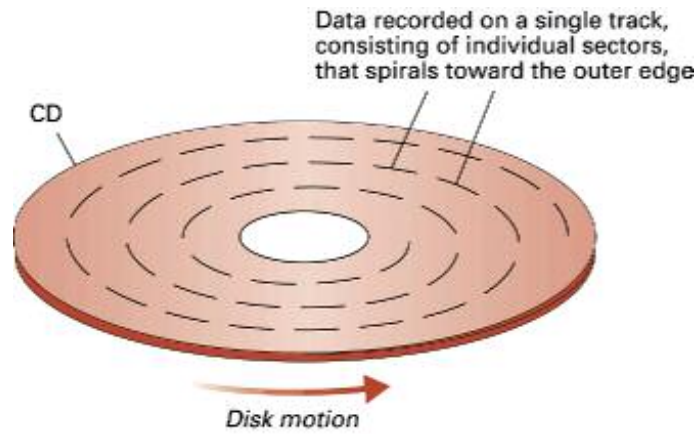
## Figure 1.9 A disk storage system



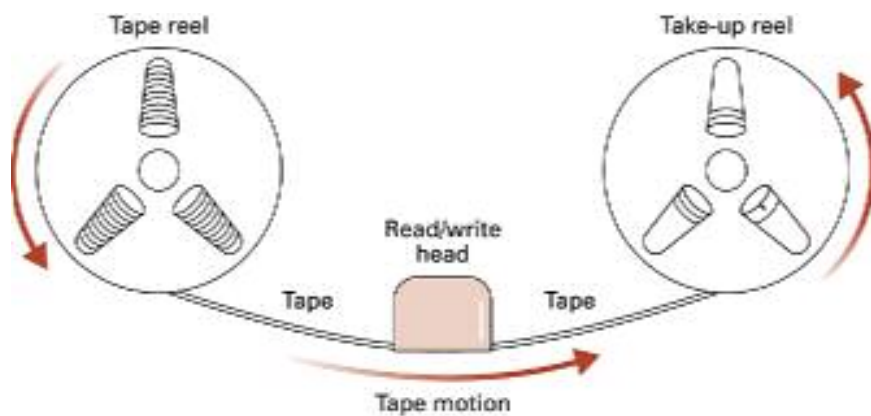




**Figure 1.10** CD storage format



**Figure 1.11** A magnetic tape storage mechanism



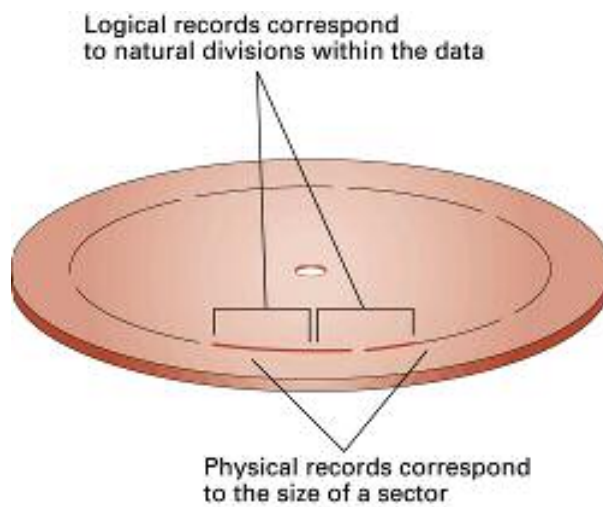


## Files

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## Figure 1.12 Logical records versus physical records on a disk





## Representing text

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## ASCII Values

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**Figure 1.13** The message “Hello.” in ASCII

01001000	01100101	01101100	01101100	01101111	00101110
H	e	l	l	o	.

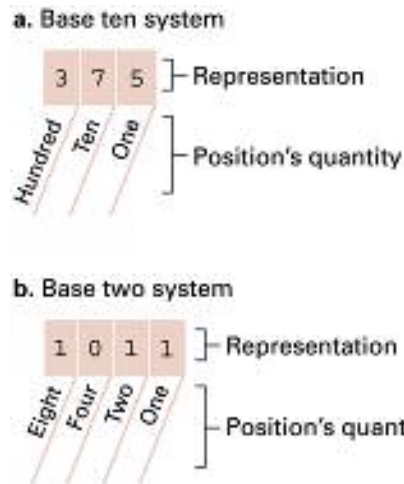


## Representing numeric values

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**Figure 1.15** The base ten and binary systems

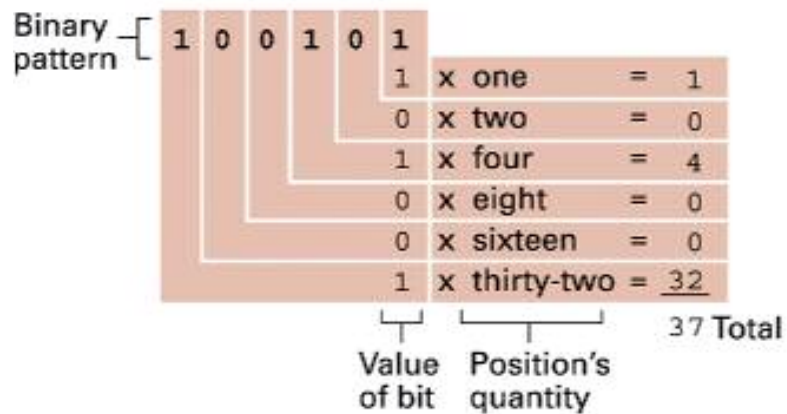


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1-25



**Figure 1.16** Decoding the binary representation 100101



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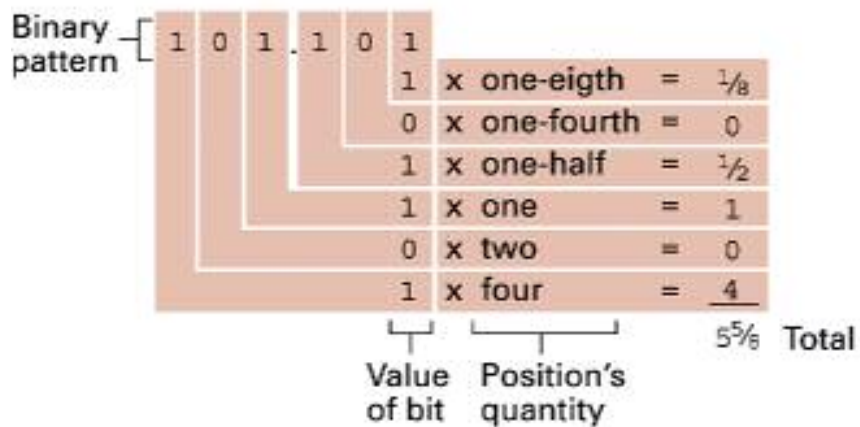


**Figure 1.19** The binary addition facts

$$\begin{array}{r} 0 \\ + 0 \\ \hline 0 \end{array} \quad \begin{array}{r} 1 \\ + 0 \\ \hline 1 \end{array} \quad \begin{array}{r} 0 \\ + 1 \\ \hline 1 \end{array} \quad \begin{array}{r} 1 \\ + 1 \\ \hline 10 \end{array}$$



**Figure 1.20** Decoding the binary representation 101.101





## Representing Integers

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## Figure 1.21 Two's complement notation systems

a. Using patterns of length three

Bit pattern	Value represented
011	3
010	2
001	1
000	0
111	-1
110	-2
101	-3
100	-4

b. Using patterns of length four

Bit pattern	Value represented
0111	7
0110	6
0101	5
0100	4
0011	3
0010	2
0001	1
0000	0
1111	-1
1110	-2
1101	-3
1100	-4
1011	-5
1010	-6
1001	-7
1000	-8



**Figure 1.22** Coding the value -6 in two's complement notation using four bits

